

Computing a complete finite prefix of the unfolding of a
I-safe net

McMillan / Esparza

- Every reachable marking is represented
- Every live transition occurs in the prefix

Configuration C

↓ closed of events, #-free

$\text{Min} \rightsquigarrow M(C)$

$\uparrow C = C' \text{ s.t. } C \leq C'$

$\forall C' \in \uparrow C, C' = C + E$



$$\text{Mark}(C_1) = \text{Mark}(C_2) \Rightarrow$$

$$\forall C_1' = C_1 + E_1 \in \uparrow C_1$$

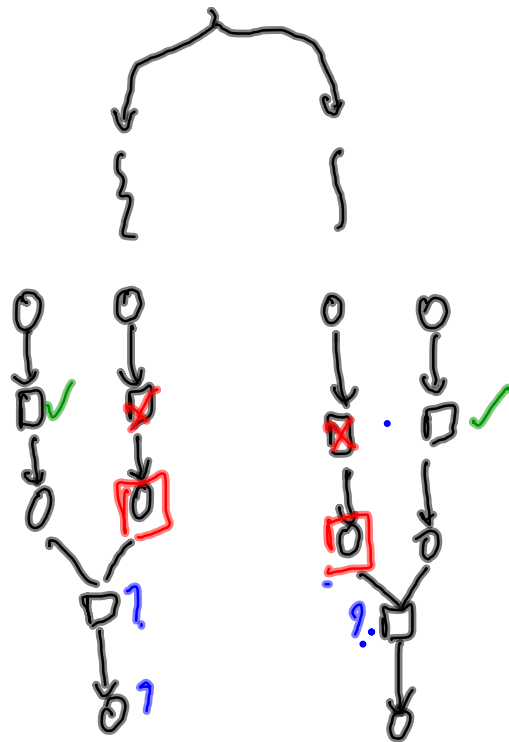
$$\exists C_2' = C_2 + E_2 \in \uparrow C_2 \quad \text{s.t.} \quad E_1 \simeq E_2$$

Isomorphism
↓

Local configurations: $[e] = \downarrow e$ (e is an event in unfolding)

$$\text{Mark}([e_1]) = \text{Mark}([e_2]).$$

- Identify one of these as a "cutoff" event - do not explore $\uparrow e$

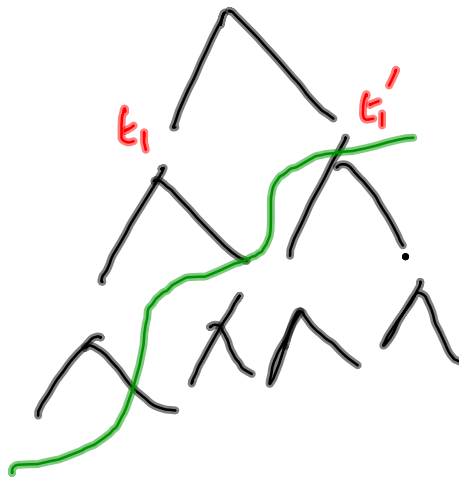
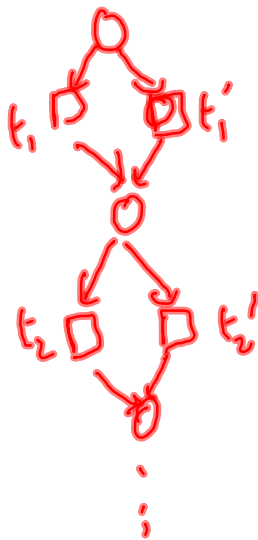


McMillan's idea

Cut off if

$$\text{Mark}(e_1) = \text{Mark}(e_2)$$

$$\& \ |e_1| < |e_2|$$



Adequate order: \prec on configuration = p.o. st.

- $C_1 \subset C_2 \Rightarrow C_1 \prec C_2$
- \prec is well founded
- $C_1 \prec C_2 \wedge \text{Mark}(C_1) = \text{Mark}(C_2)$
 $\forall E_1, C_1 + E_1 \prec C_2 + I(E_1)$

Unfold, at each point explore e st. $[e]$ is
of minimal among enabled events

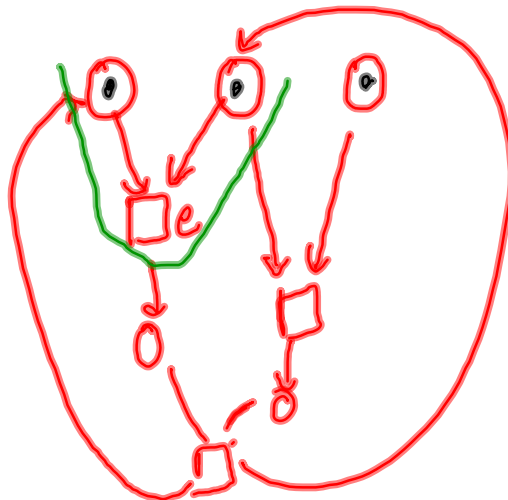
Cutoff event e' is a cutoff event if $\exists e$ in
the prefix already constructed st.

$$\text{Mark}(e) = \text{Mark}(e')$$

$$\< [e] < [e']$$

This unfolding strategy generates a finite prefix
that is complete

Finiteness: Along any path, if we see $2^n + 1$ copies of e , two of them must agree on $\text{Mark}(e)$.



$m = \# \text{ reachable markings}$

Any sequence of $m+1$ events generates a
cut off event

$\Rightarrow \text{depth (unfolding)} \leq m+1$

Prove that $\# \text{ places is finite}$

Completeness

Suppose $M \in \text{Reach}(Min)$ is not represented.

$\exists C$ in inf. unif s.t. $\text{Mark}(C) = M$

$\therefore C$ contains some cutoff event $e \in C$

$\therefore C = [e] + E$

e cutoff by $e' \Rightarrow C' = [e'] + E$ has same marking
 $C' < C$ since $[e'] < [e]$

Repeat arg for C' not present in Fin

Find $C'' < C'$ Contradiction because $<$
 is well founded

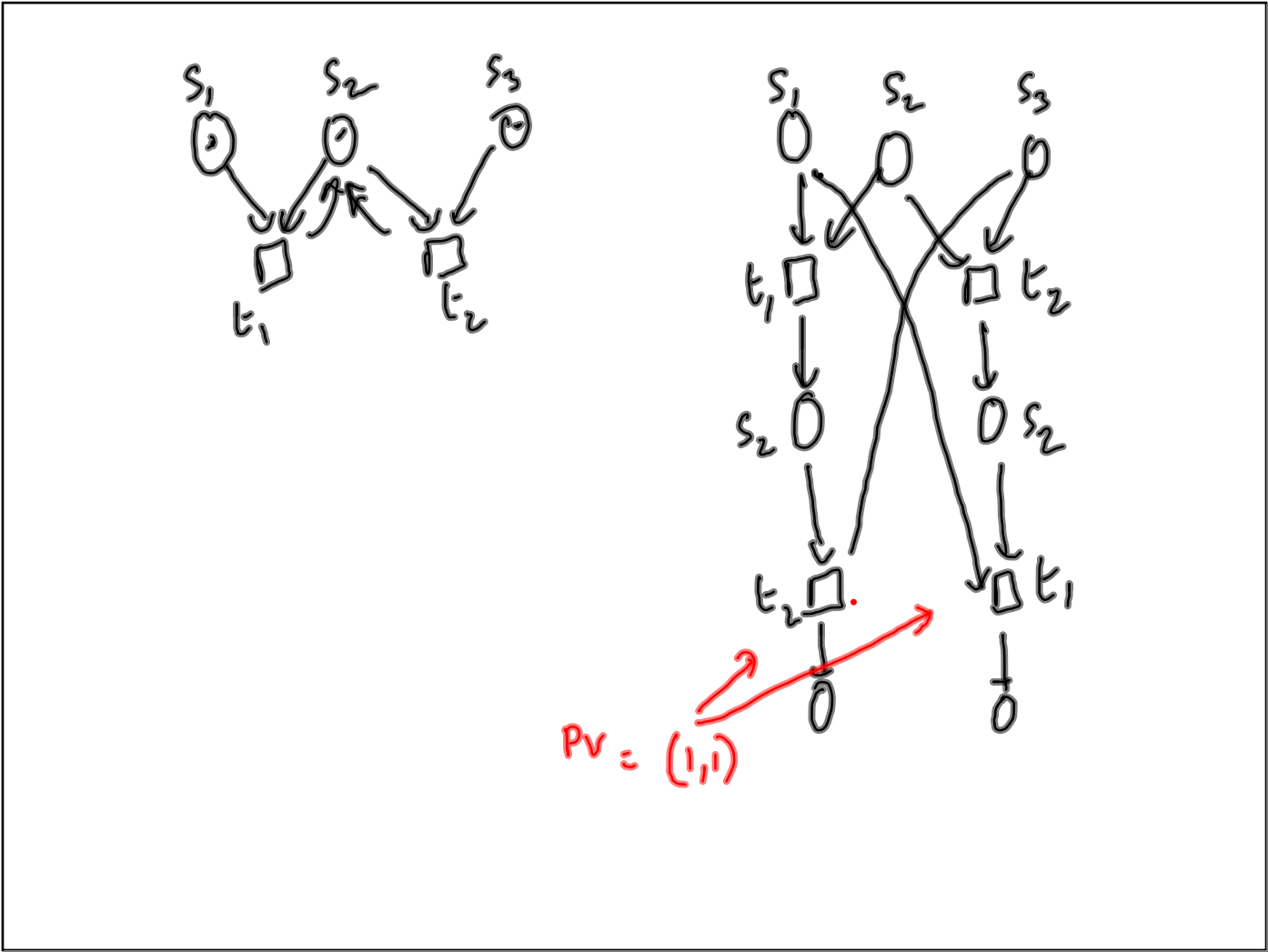
An improved adequate order

$$C_1 <_E C_2 \text{ if } |C_1| < |C_2|$$

$$\text{or } |C_1| = |C_2| \&$$

fix a linear order
on transitions in
original net $\rightarrow \text{Parikh Vector}(C_1) <_{\mathbb{N}} \text{Parikh Vector}(C_2)$

Claim: This is an adequate order



"Total" adequate order

Whenever we construct F_{in} using \prec .

if we explore e' & $\text{Mark}(e') \neq \text{Mark}(e)$

for some existing e , then $e \prec e'$

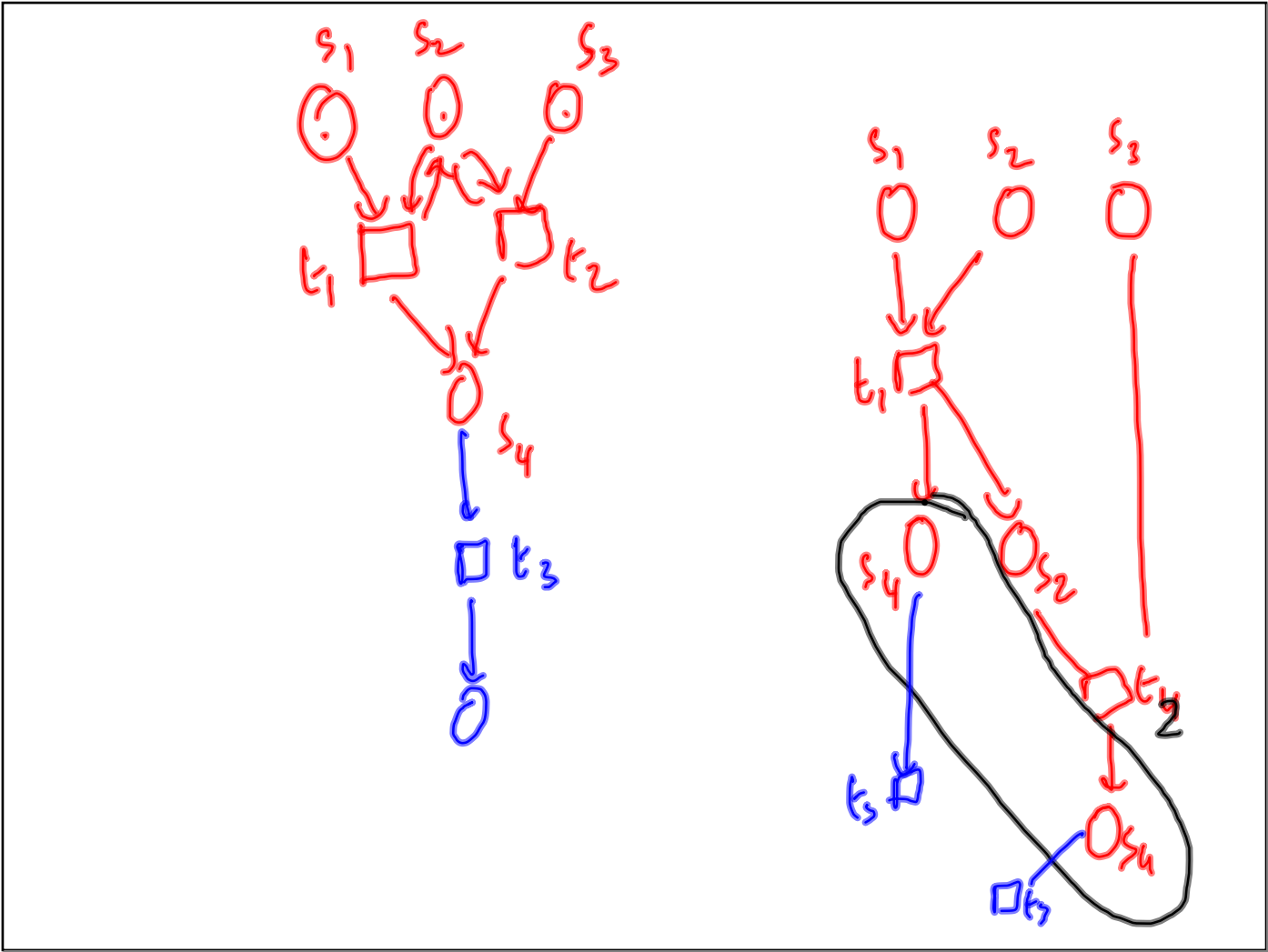
\prec_E Size McMillan
 \prec_F { + Parikh Vector
 + Parikh Vector on max step decomposition
 = Foata Normal Form

$T = (E, \prec, \lambda)$ Minimal element of trace = Step 1

Delete min element & iterate

Show that \prec_F is adequate and total

Crucially uses 1-safeness



Timed Systems

Incorporate time into automata/languages

Abstractly: Behavior is a word $w \in \Sigma^*$

Action a_i is done at t_i

$w = a_1 a_2 a_3 \dots a_k$

$t_1 \leq t_2 \leq t_3 \dots \leq t_k \in \mathbb{R}$

Infinite behaviour \Rightarrow time should "progress"

$\forall r \in \mathbb{R} \exists i \ t_i > r$

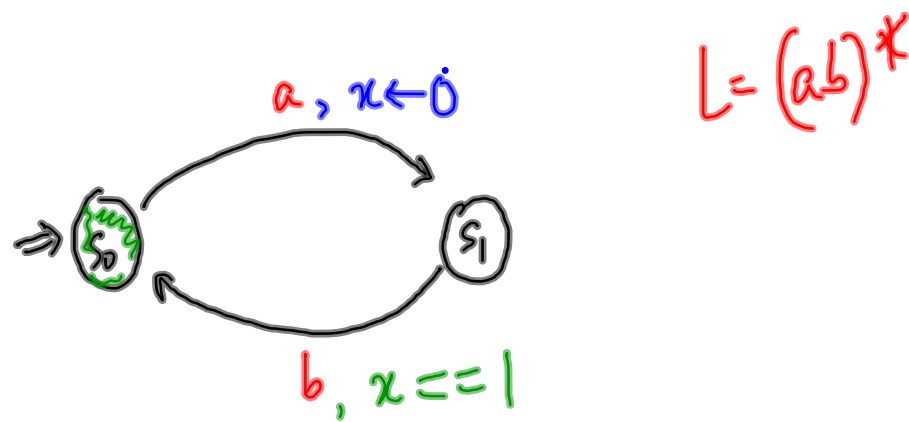
Timed Word: (w, σ)

Pair of sequences, or a sequence of pairs
 $(a_1, t_1), (a_2, t_2) \dots (a_n, t_n)$

All timed words where each a at time t is
 followed by a b at time $t+1$

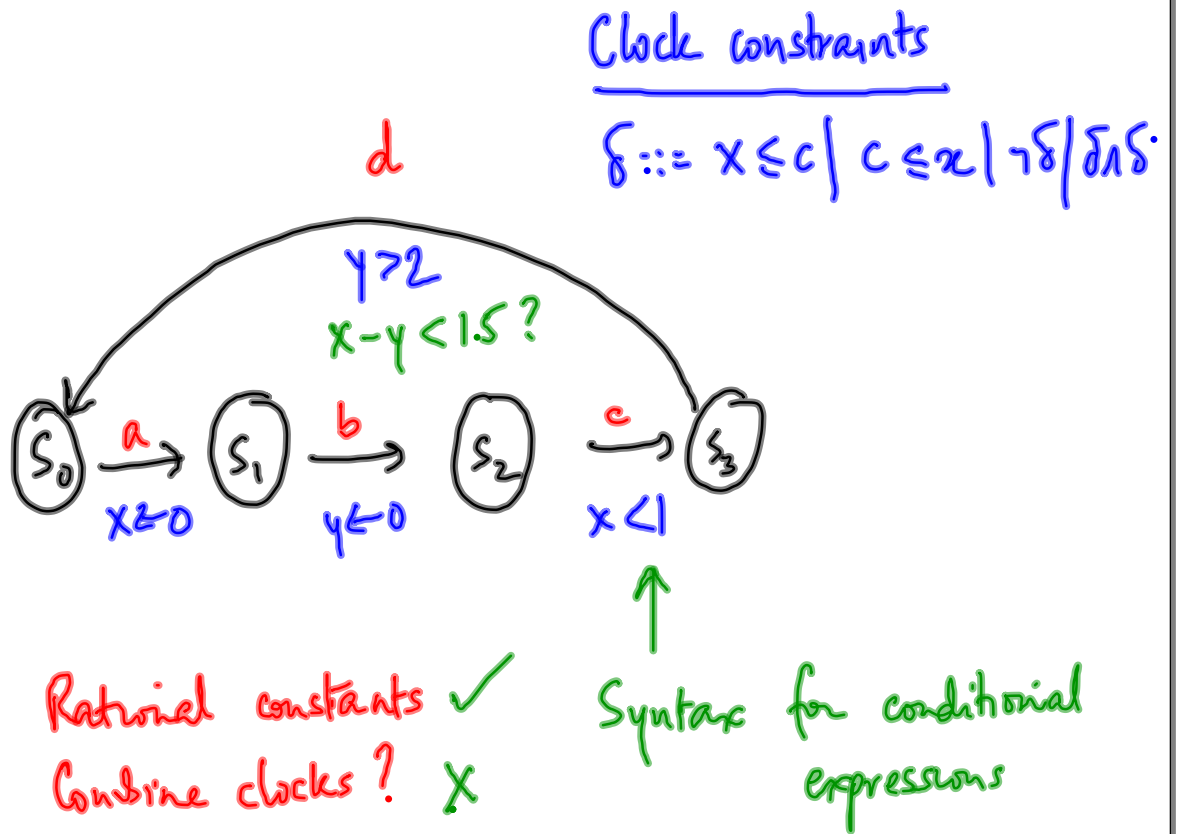
Alur & Dill Add special variables called "clocks"
 to finite state automata

- implicitly "grow" as time progresses
- clocks can be reset (to 0)
- conditional transitions based on clock values



$(a, t_1), (b, t_2), (a, t_3), (b, t_4), \dots$

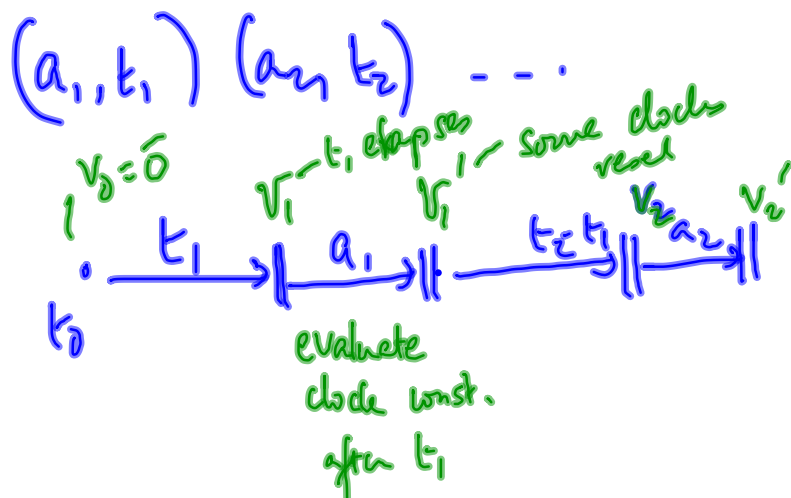
s.t. $\forall \text{ odd } i \quad t_{i+1} - t_i = 1$



$C = \text{set of clocks (finite)}$
 Clock valuation: $v: C \rightarrow \mathbb{R}_{\geq 0}$

$v \models \varphi$, φ is a clock constraint

Wrt clock valuation v , clock constraint φ is true

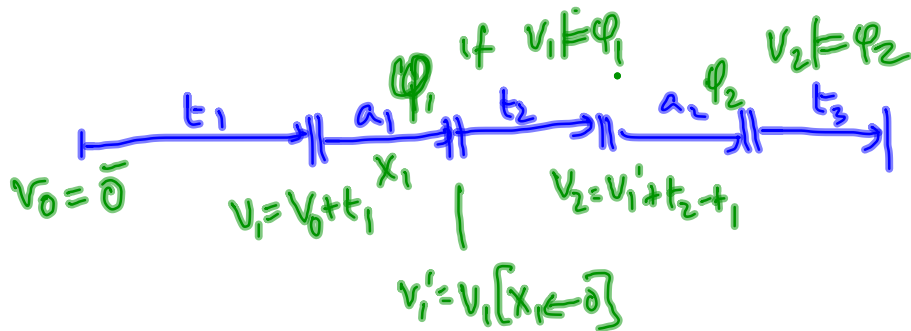


Operations on valuations

$$\underbrace{v + t}_{\text{new value}}(c) = v(c) + t \quad \forall c \in C$$

Given $X \subseteq C$ & $r \in \mathbb{R}_{\geq 0}$

$$v[X \leftarrow r](c) = \begin{cases} v(c) & \text{if } c \notin X \\ r & \text{if } c \in X \end{cases}$$



Timed Automaton over Σ

$$TA = (Q, Q_{in}, F, C, \rightarrow)$$

set of constraints
wrt a set
of clocks C

$$\rightarrow \subseteq Q \times Q \times \Sigma \times 2^C \times \overline{\Phi}(C)$$

from
to
act
reset
constraint

↓
finite

$$q \xrightarrow[a, \varphi]{\text{act} \quad \text{const.}} q'$$

X
reset

Run of TA on a timed word (w, σ)



Sequence of configurations

$= (a_1, t_1) (a_2, t_2) \dots (a_n, t_n)$

$$(q_{in}, \bar{0}) \xrightarrow[t_1]{a_1} (q_1, v_1) \xrightarrow[t_2]{a_2} (q_2, v_2)$$

↓
 $\in Q_{in}$
 ↓
 zero
 valuation

$$\text{if } \exists \quad q_{in} \xrightarrow[x]{a_1, \varphi} q_1$$

$$\text{s.t. } v_1' = \bar{0} \# t_1 \models \varphi$$

$$v_1 = v_1' [x \leftarrow \bar{0}]$$

$$q_1 \xrightarrow[x']{a_2, \varphi'} q_2$$

$$v_2' = v_1' + (t_2 - t_1) \models \varphi'$$

$$v_2 = v_2' [x' \leftarrow 0]$$

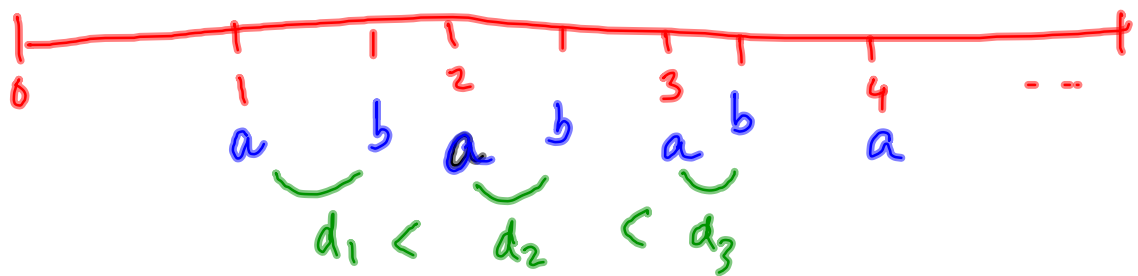
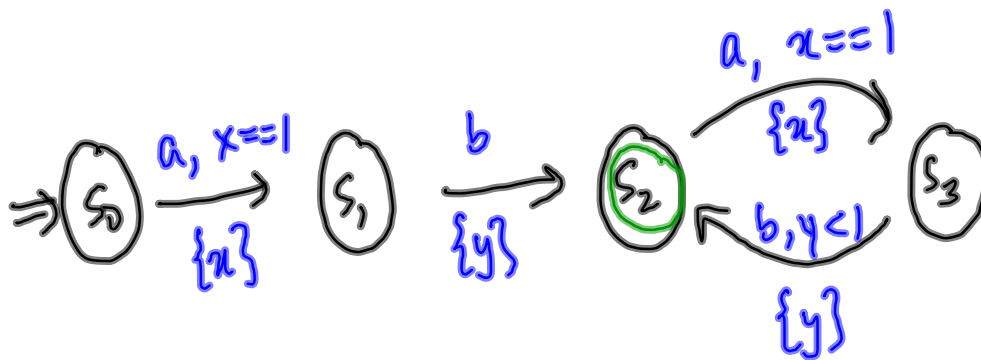
$$(q_0, \vec{0}) \xrightarrow[t_1]{a_1} (q_1, v_1) \rightarrow \dots \xrightarrow[t_k]{a_k} (q_k, v_k)$$

Run is accepting if $q_k \in F$

$$L(TA) = \{ (w, \sigma) \mid TA \text{ has an acc. run on } (w, \sigma) \}$$

A set of timed words L is a timed regular lang
if $\exists TA$ s.t. $L = L(TA)$

Time is global



Closure under

Union ✓

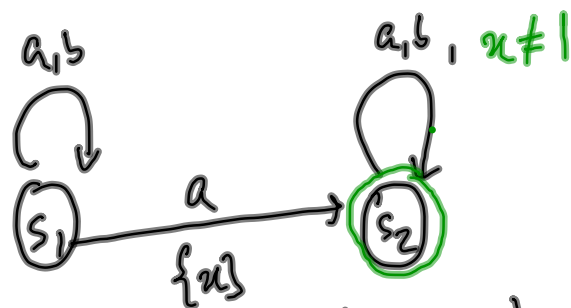
Intersection **Product** over $G_1 \cup G_2$

$$q_1 \xrightarrow[x_1]{a, \varphi_1} q'_1$$

$$q_2 \xrightarrow[x_2]{a, \varphi_2} q'_2$$

$$(q_1, q_2) \xrightarrow[x_1 \cup x_2]{a, \varphi_1 \wedge \varphi_2} (q'_1, q'_2)$$

NST closed under complementation



$L = \exists a$ s.t no action happens 1 unit after a

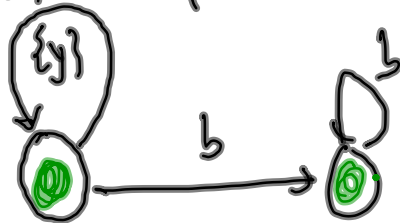
$\bar{L} = \forall a \exists$ action 1 unit after a

L' of the form a^+b^*

- all a 's happen before $t=1$

- no two a events happen at the same time

$a, x < 1 \wedge y > 0$



$\text{Untime}(L)$ = strip timing from set of
timed words

$$(w, \sigma) \longrightarrow w$$

Claim: For all timed regular lang L ,

$\text{Untime}(L)$ is regular

Use this to show \bar{L} is not timed regular