An automaton over data words that captures EMSO logic

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Data words

finite words over $\Sigma \times D^m$

finite

label

infinite

data values

$m \geq 0$

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	finite	infinite	$m \geq 0$
	label	data values	
XML	tag	contents	$m = 1$

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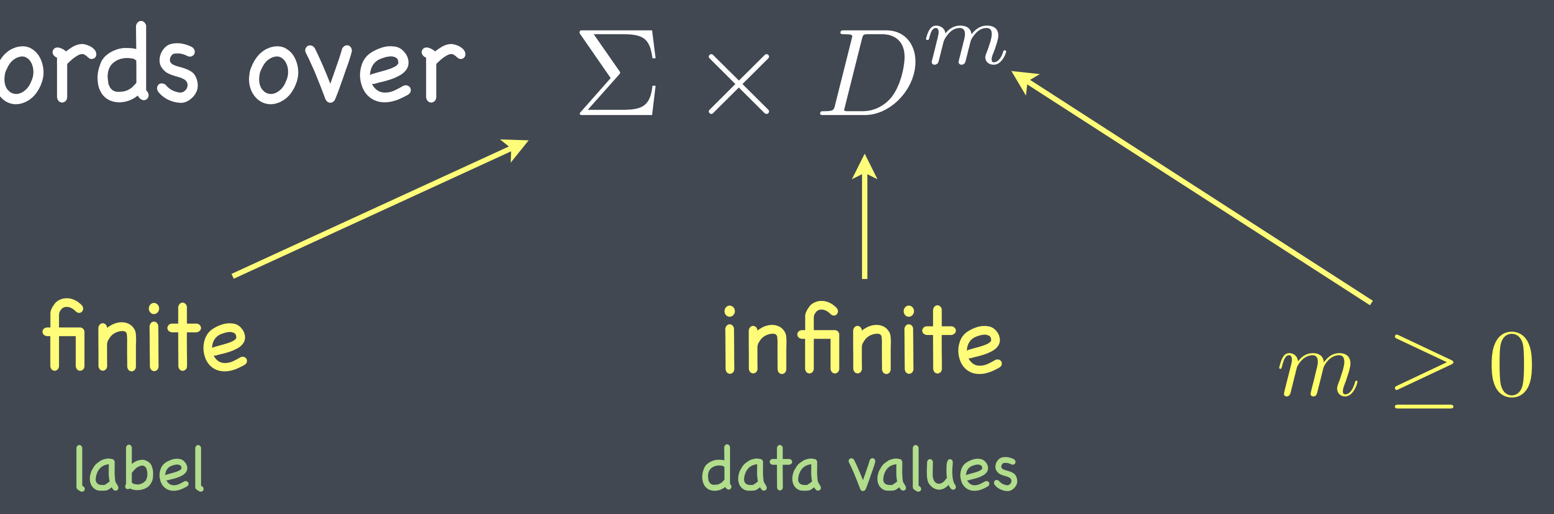
XML	tag	contents	$m = 1$
time	action	$\mathbb{R}^{\geq 0}$	$m = 1$

Data words



finite words over $\Sigma \times D^m$

finite

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data values

$m \geq 0$

XML	tag	contents	$m = 1$
time	action	$\mathbb{R}^{\geq 0}$	$m = 1$
messages	{ ! , ? , fork }	$\mathbb{N}$	$m = 2$

fork	fork	!	?	!	?
1	2	2	1	1	3
2	3	1	2	3	1

Automata vs. Logic

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- Logic
  - Specifying properties
  - Declarative (what should happen)

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Looking for an expressive logic with reasonable implementation model (one-way, non-deterministic)

Logic

MSO logic for data words

- $a(x)$ position x carries $a \in \Sigma$
- $x \prec_{+1} y$ y is direct successor of x
- $\varphi_1 \vee \varphi_2$ $\neg\varphi$ $\exists x \varphi$ $\exists X \varphi$ $x \in X$

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- $d^k(x) = d^l(y)$ k-th data value at x equals l-th data value at y

  $k, l \in \{1, \ldots, m\}$

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- $d^k(x) = d^l(y)$ ~~k-th data value at x~~ equals l-th data value at y

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too expressive

=> restrict access to data values

=> relate positions that automaton can access

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  for all i there is at most one j such that $j \lhd^w i$
- monotonicity

$$i \lhd^w j \;\wedge\; i' \lhd^w j' \;\wedge\; w_i = w_{i'} \;\wedge\; w_j = w_{j'}$$

$$\Longrightarrow \quad i < i' \quad \text{iff} \quad j < j'$$

MSO logic for data words

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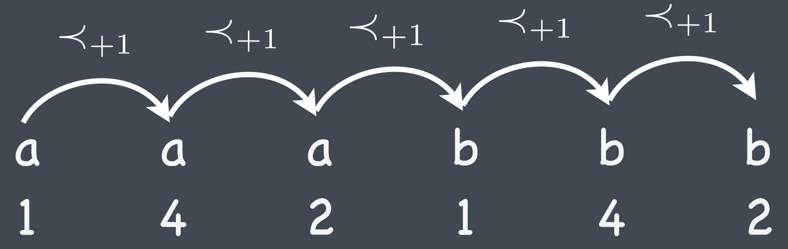
- direct successor relation $\prec_{+1}$



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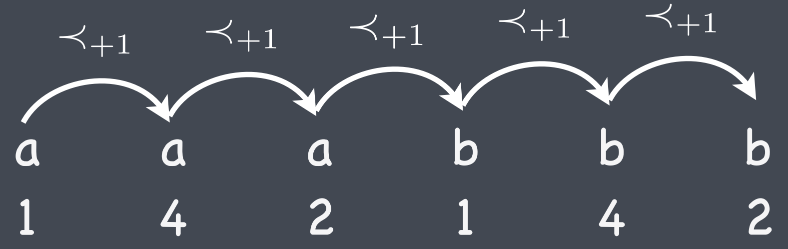
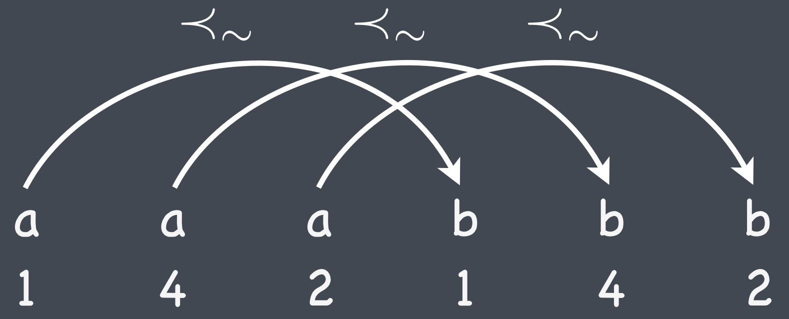


- successive positions with the same data value $\prec_{\sim}$



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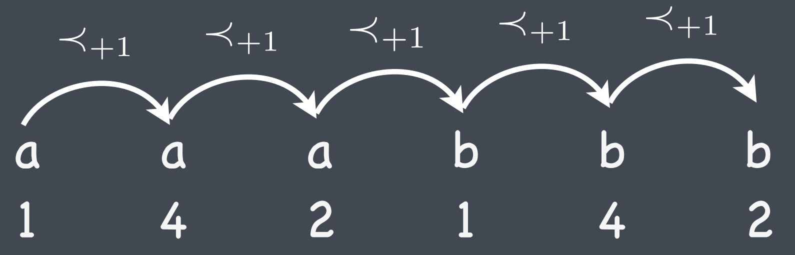

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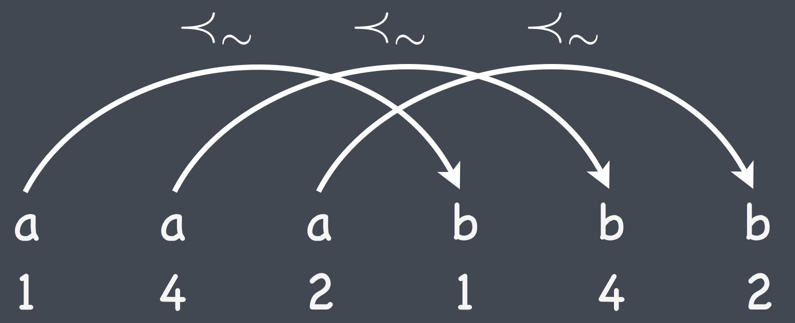
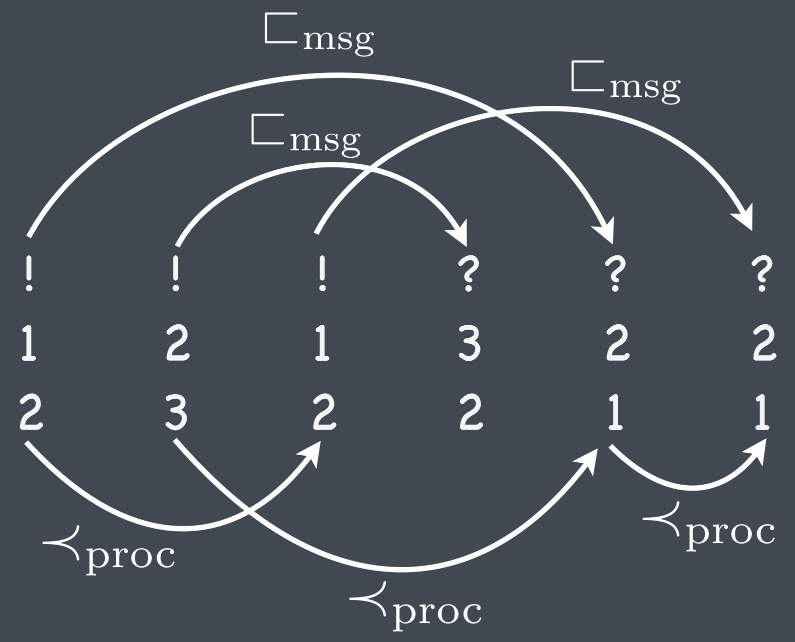


- message-passing system (m=2)



EMSO(S)

where S is any signature

- $a(x)$ position x carries $a \in \Sigma$
- $x \lhd y$ $\lhd \in$ S
- $d^k(x) = d^l(x)$ local reasoning about data values
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Formula: $\exists X_1 \ldots \exists X_n \varphi$

first-order

Example formulas (m=1)

req	req	req	ack	ack	req
4	4	2	1	4	2

Example formulas (m=1)

- there is a request that is acknowledged

$$\exists x \exists y \, (req(x) \wedge ack(y) \wedge x \precsim y)$$

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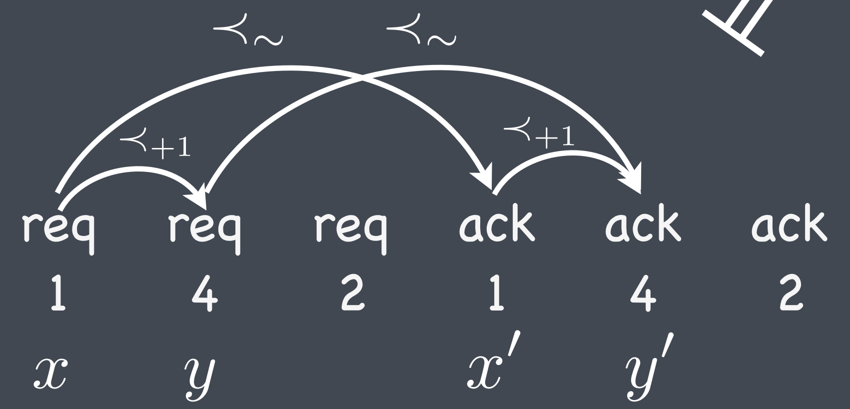

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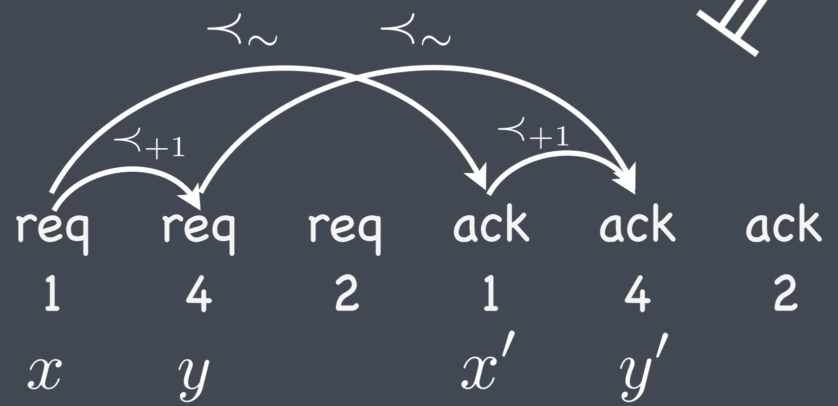
$\Dashv$



Goal:
non-deterministic
one way automaton for
this kind of property

From Logic to Automata

[related works, most of them for m=1]

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- EMSO(S) → ? (non-deterministic, one-way)
  (e.g., $\text{EMSO}(\prec_\sim, \prec_{+1})$)

Automata

Register Automata

[Kaminski & Francez, 1994]

$$\mathcal{A} = (Q, R, \longrightarrow, q_0, F)$$

- Q finite set of states
- q_0, F initial state, set of final states

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$$guard \in \mathcal{B}(R)$$

current value is in 1st but not in 2nd register:

$$r_1 \wedge \neg r_2$$

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$$guard \in \mathcal{B}(R) \qquad upd \subseteq R$$

current value is in 1st but not in 2nd register:

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write current value in both registers:

$$\{r_1, r_2\}$$

Register Automata

[Kaminski & Francez, 1994]

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$D = \mathbb{N}$

$F = \{q_1\}$

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q_0		req	q_0	$\{r\}$
q_0	r	ack	q_1	
q_1		req , ack	q_1	

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req	req	ack	req	ack	ack	ack	req
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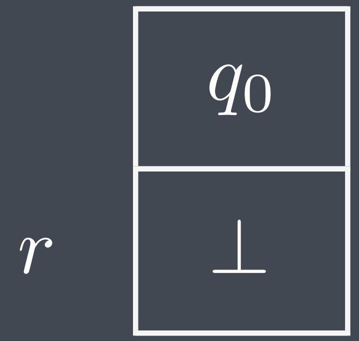

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r	$\perp$	$\perp$	5
		→	⬇

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		→	⬇	→

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=> class memory automata

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		→	⬇	→	⬇	→	✔	⇒	⇒

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~~R~~	~~finite set of registers~~

Class Memory Automata

[Björklund & Schwentick, 2007]

$$A = (Q, \cancel{R}, \longrightarrow, q_0, F)$$

- Q finite set of states
- q_0 initial state
- ~~R finite set of registers~~
- transition relation:

$$\begin{tikzcd} p \arrow[rr, bend left, "\precsim"] & q \arrow[r, "a"] & q' \end{tikzcd}$$

q is current state
p is state after last position with same data value

Class Memory Automata

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$$q \xrightarrow{a} q'$$

q is current state
data value occurs for the first time

Class Memory Automata

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- ~~R finite set of registers~~
- transition relation:

$$\begin{tikzcd} p \arrow[rr, bend left, "\prec_\sim"] & q \arrow[r, "a"] & q' \end{tikzcd}$$

q is current state
p is state after last position with same data value

$$q \xrightarrow{a} q'$$

q is current state
data value occurs for the first time

- $F = (F_\sim, F_{+1})$ sets of final states

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
q_0	q_0		ack	q_1	
q_0	q_1		ack	q_1	

$F_\sim = \{q_1\}$

$F_{+1} = \{q_1\}$

$L(\mathcal{A}) =$ " every process sends one request, which is acknowledged,
every acknowledgment is preceded by a request, and req*ack* "

Class Memory Automata

[Björklund & Schwentick, 2007]

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$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
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req	req	req	req	ack	ack	ack	ack
8	5	3	4	3	4	5	8

$\boxed{q_0}$

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
q_0	q_0		ack	q_1	
q_0	q_1		ack	q_1	

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	req	req	req	req	ack	ack	ack	ack
	8	5	3	4	3	4	5	8
q_0	q_0							

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
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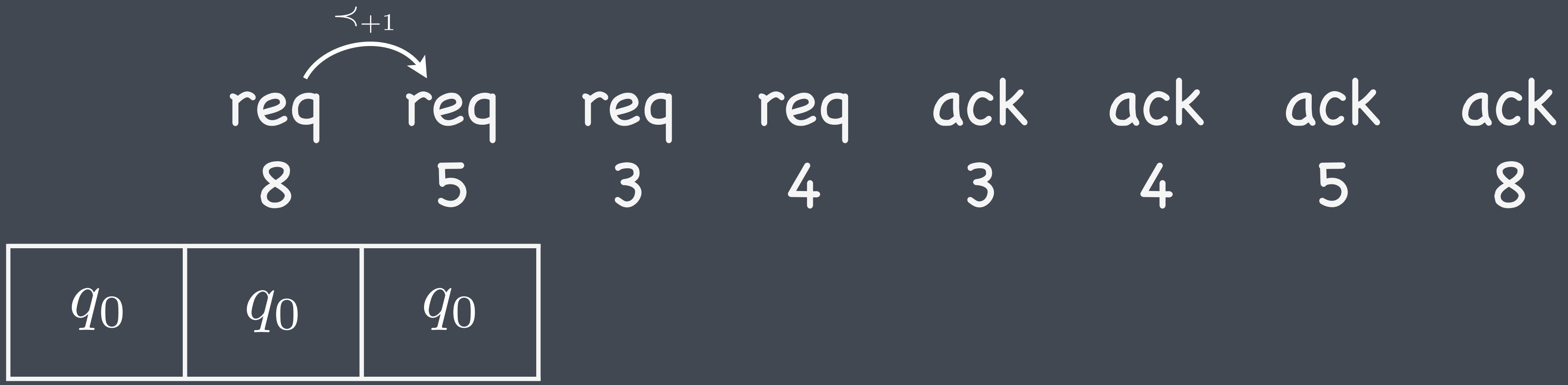

Class Memory Automata

[Björklund & Schwentick, 2007]

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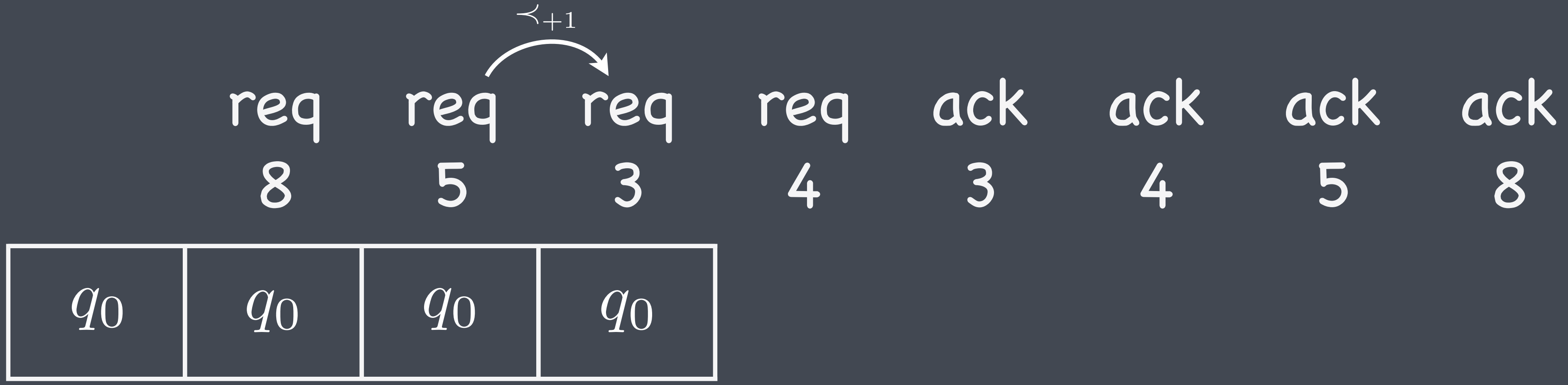

req	req	req	req	ack	ack	ack	ack
8	5	3	4	3	4	5	8

q_0	q_0	q_0	q_0

Class Memory Automata

[Björklund & Schwentick, 2007]

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$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
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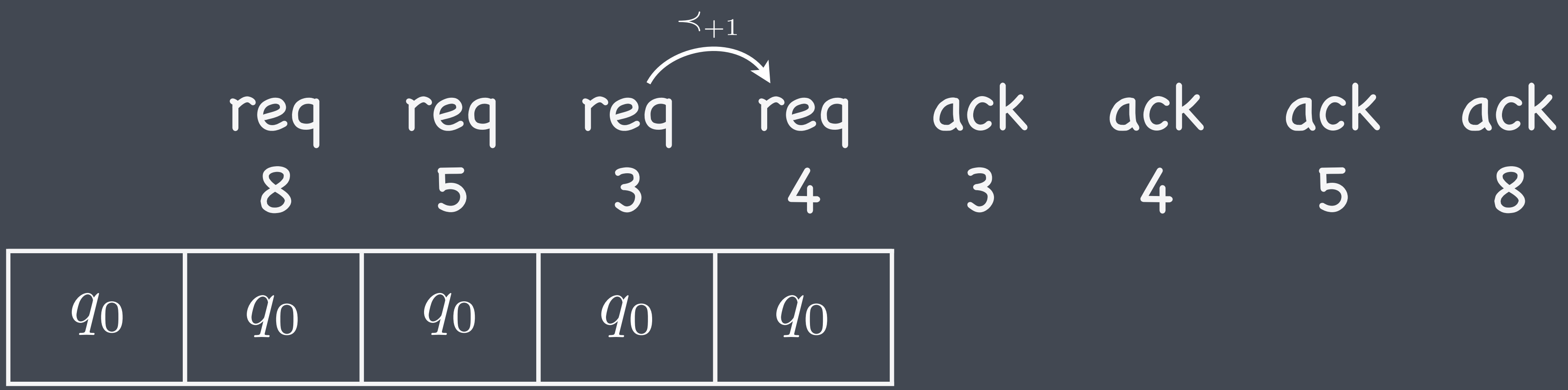

	req	req	req	req	ack	ack	ack	ack
	8	5	3	4	3	4	5	8
q_0	q_0	q_0	q_0	q_0				

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
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q_0	q_0		ack	q_1	
q_0	q_1		ack	q_1	

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8	5	3	4	3	4	5	8

q_0	q_0	q_0	q_0	q_0	q_1

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

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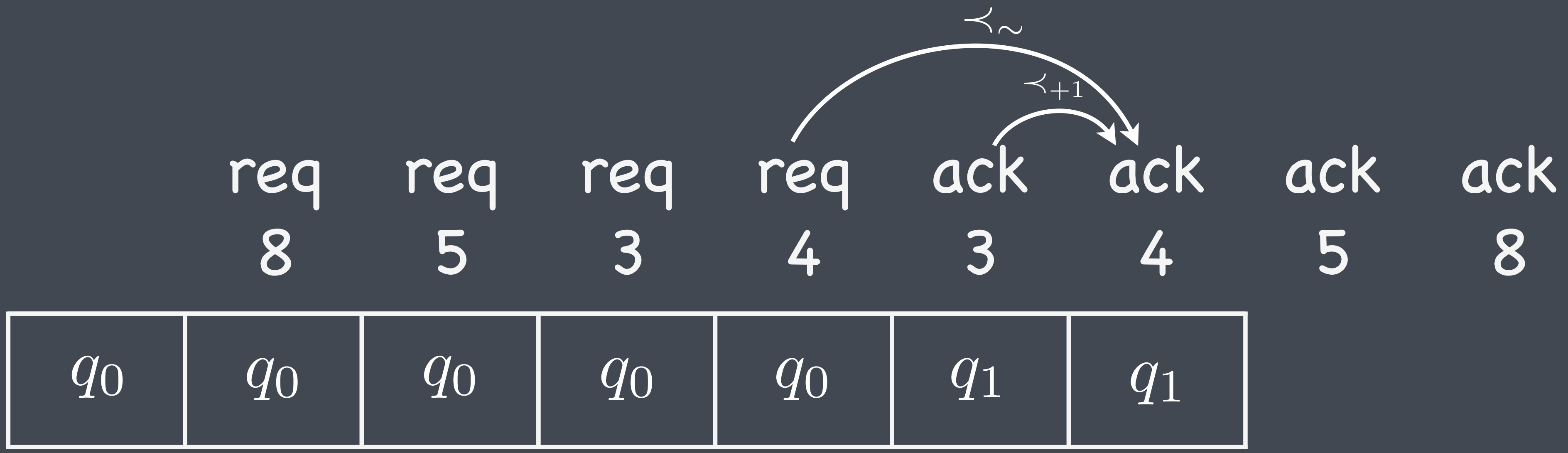

Class Memory Automata

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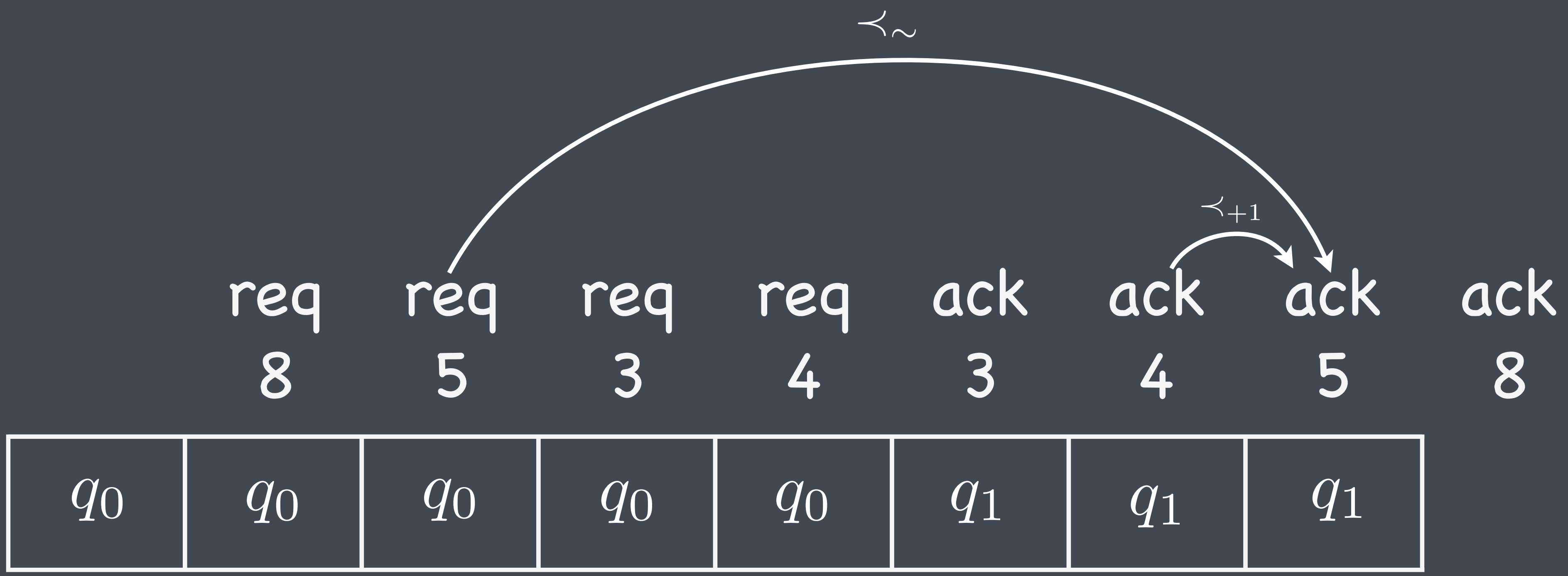

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
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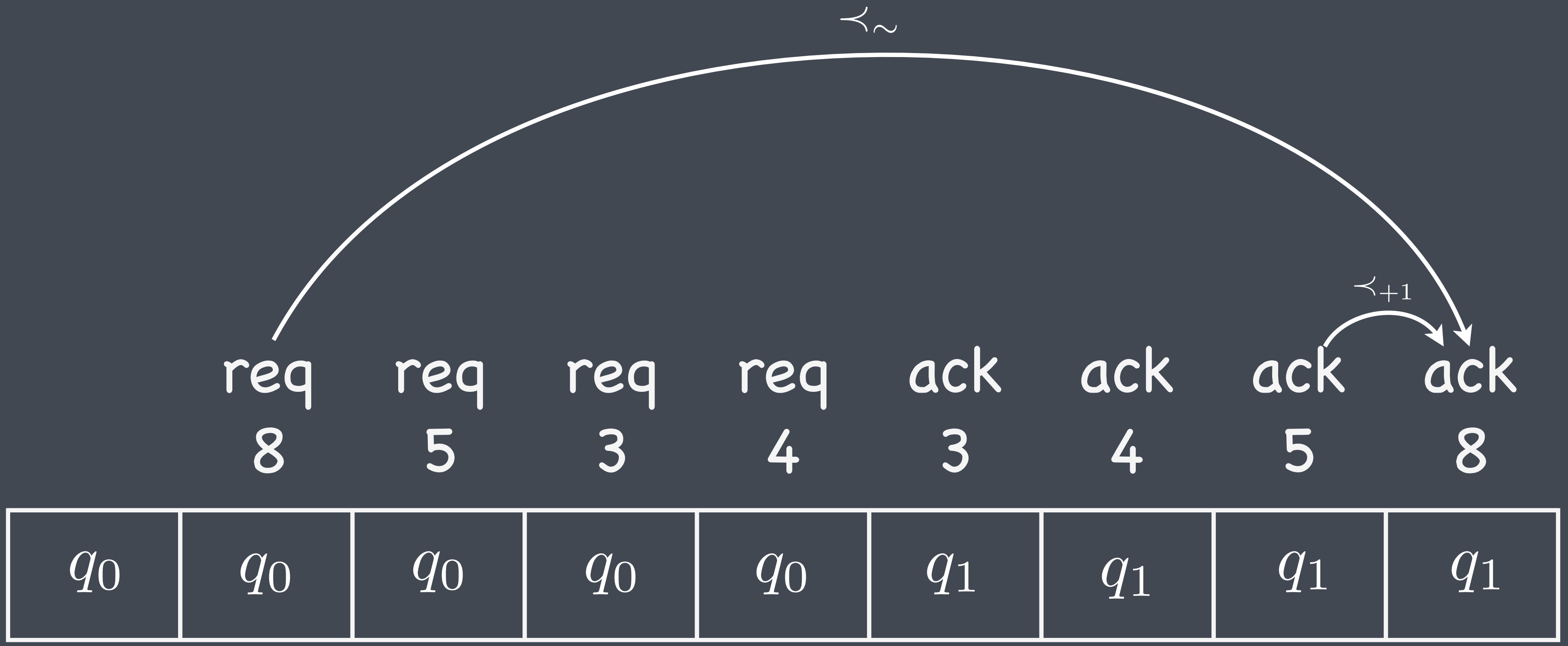

	req	req	req	req	ack	ack	ack	ack
	8	5	3	4	3	4	5	8
q_0	q_0	q_0	q_0	q_0	q_1	q_1	q_1	q_1

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_{\sim}$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
q_0	q_0		ack	q_1	
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... and requests are acknowledged in the order they are received ?

req req req req ack ack ack ack

8 5 3 4 3 4 5 8

q_0	q_0	q_0	q_0	q_0	q_1	q_1	q_1	q_1

Class Memory Automata

[Björklund & Schwentick, 2007]

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	~~guard~~	label	target	~~update~~
	q_0		req	q_0	
q_0	q_0		ack	q_1	
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... and requests are acknowledged in the order they are received ?

=> class register automata

	req	req	req	req	ack	ack	ack	ack
	8	5	3	4	3	4	5	8
q_0	q_0	q_0	q_0	q_0	q_1	q_1	q_1	q_1

Class Register Automata

over S = $\{\lhd_1, \ldots, \lhd_n\}$

$$A = (Q, \xcancel{R}, \longrightarrow, q_0, F)$$

- Q finite set of states
- ~~R finite set of registers~~
- transition relation:

Class Register Automata

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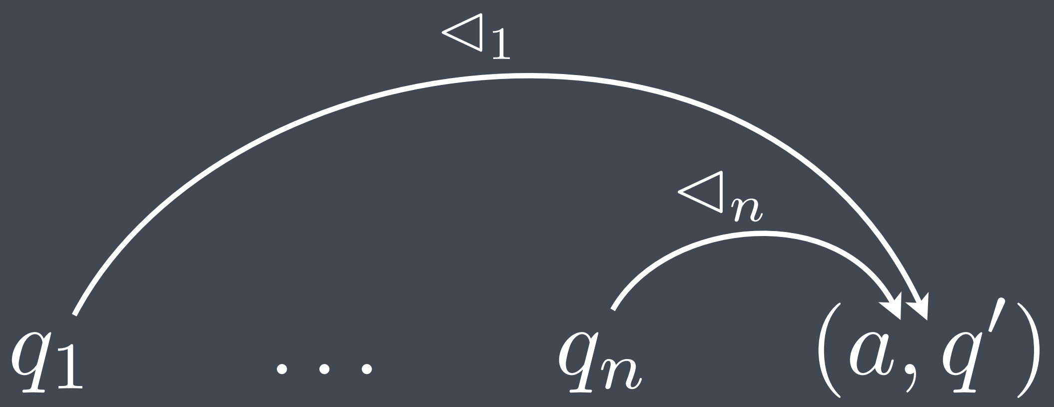

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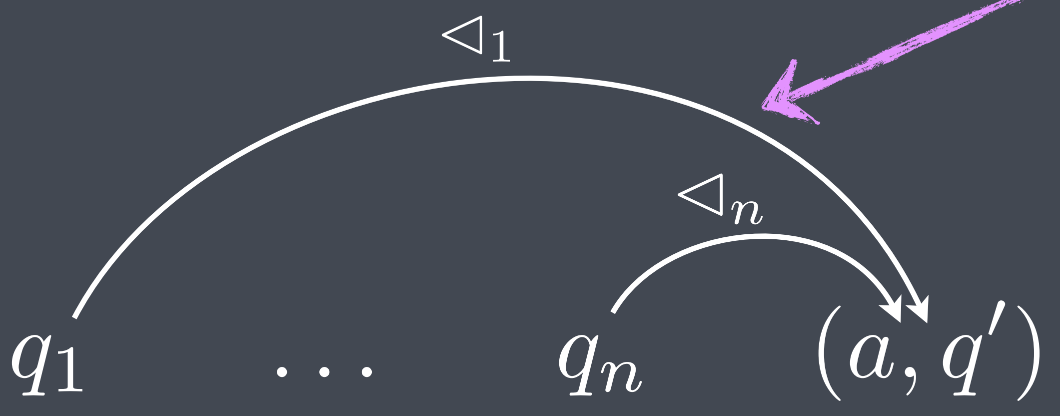

can be missing

Class Register Automata

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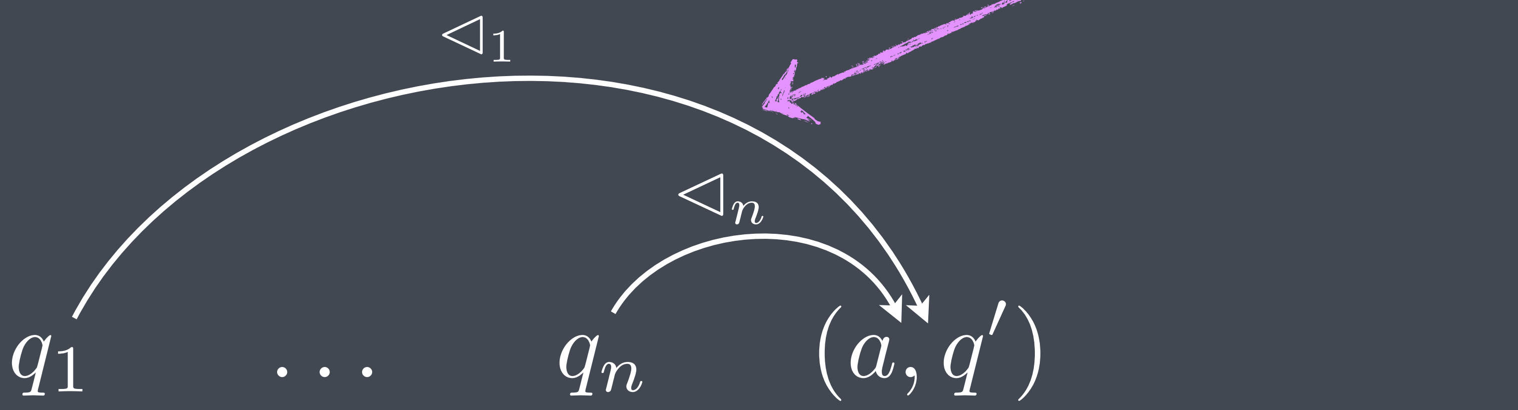

Class Register Automata

over S = $\{\lhd_1, \dots, \lhd_n\}$

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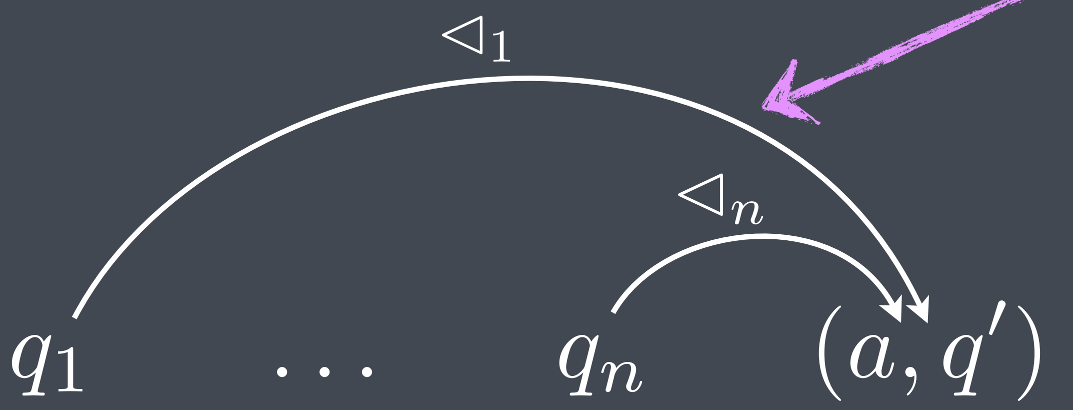
- transition relation:

- $F = (F_{\lhd_1}, \dots, F_{\lhd_n})$



can be missing

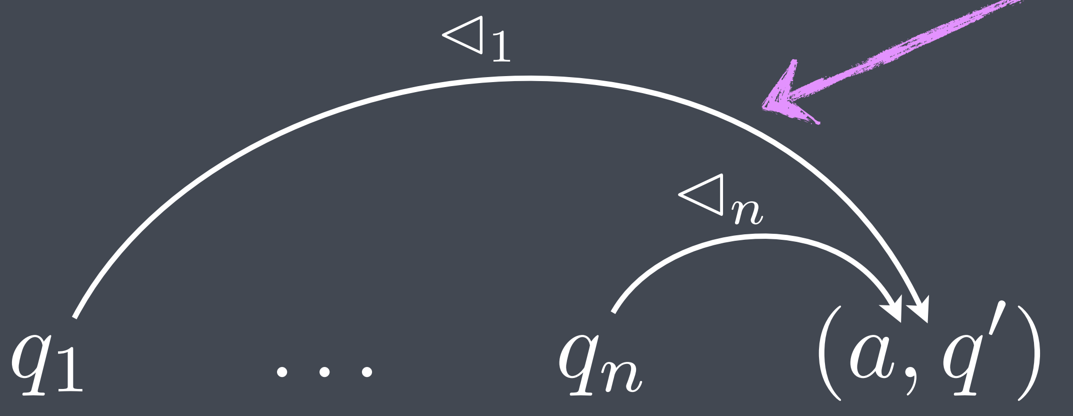
Class Register Automata

over S = $\{\lhd_1, \ldots, \lhd_n\}$

$$\mathcal{A} = (Q, \cancel{R}, \longrightarrow, \cancel{q_0}, F)\ G$$

- Q finite set of states
- ~~R finite set of registers~~
- transition relation:

- $F = (F_{\lhd_1}, \ldots, F_{\lhd_n})$
- $G \in \mathcal{B}(\text{“}q \leq N\text{”})$



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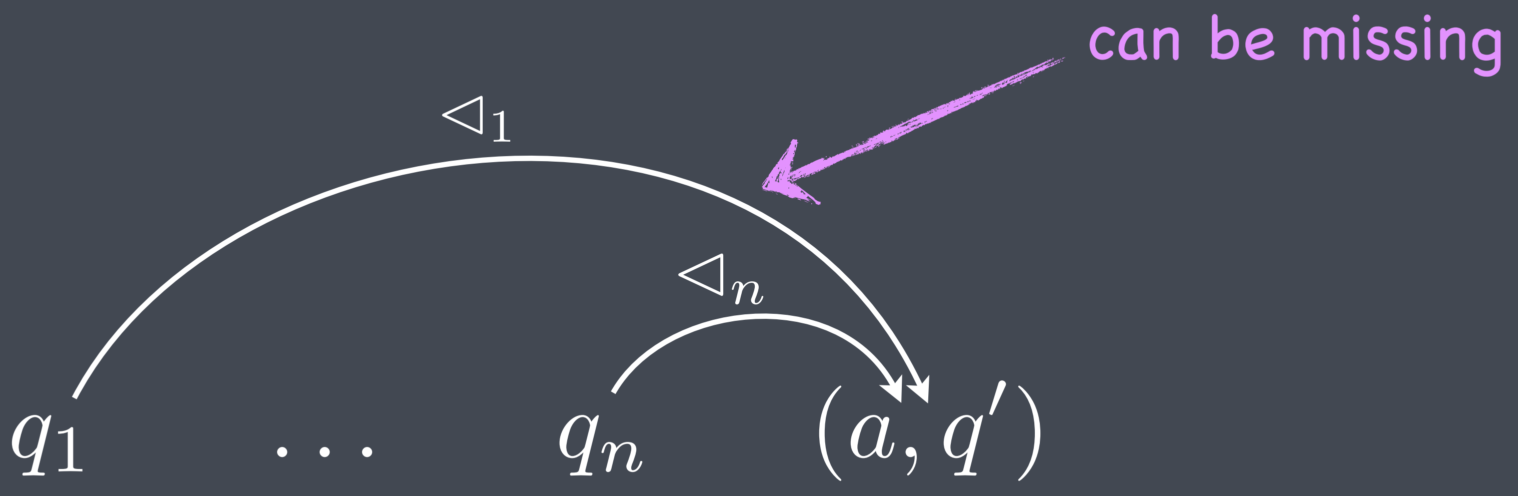

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- $G \in \mathcal{B}(\text{“}q \leq N\text{”})$

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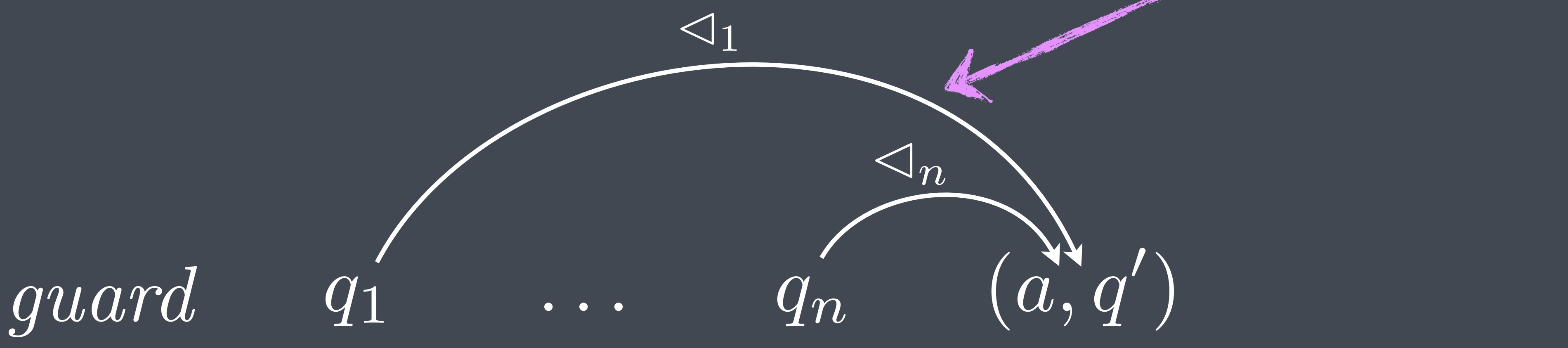

can be missing

$guard \in \mathcal{B}(((S \times R) \cup \{1, \ldots, m\})^2)$

contents of r_1 at $\lhd_1$ = contents of r_2 at $\lhd_2$

$(\lhd_1, r_1) = (\lhd_2, r_2)$

Class Register Automata

over S = $\{\lhd_1, \ldots, \lhd_n\}$

$$\mathcal{A} = (Q, R, \longrightarrow, \cancel{q_0}, F)\ G$$

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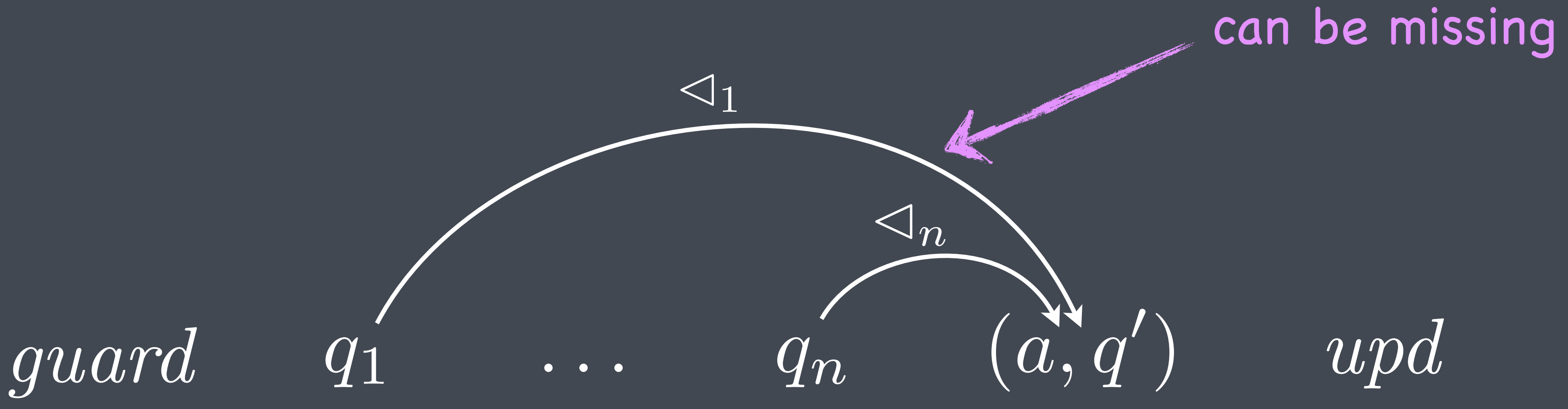

$guard \in \mathcal{B}(((S \times R) \cup \{1, \ldots, m\})^2)$

contents of r₁ at $\lhd_1$ = contents of r₂ at $\lhd_2$

$(\lhd_1, r_1) = (\lhd_2, r_2)$

$upd : R \rightharpoonup ((S \times R) \cup \{1, \ldots, m\})$

new value of r₁ := value of r₂ at $\lhd_2$

$upd(r_1) = (\lhd_2, r_2)$

Class Register Automata

$\mathcal{A}$

$F_\sim = \{q_1\}$

$F_{+1} = \{q_1\}$

$G = true$

$\prec_\sim$	$\prec_{+1}$	guard	input	target	update
			(req , d)	q_0	$r_1 := d$
	q_0		(req , d)	q_0	$r_1 := d \quad r_2 := (\prec_{+1}, r_1)$
q_0	q_0	$(\prec_\sim, r_2) = \perp$	(ack , d)	q_1	$r_1 := d$
q_0	q_1	$(\prec_\sim, r_2) = (\prec_{+1}, r_1)$	(ack , d)	q_1	$r_1 := d$

$L(\mathcal{A}) =$ " every process sends one request, which is acknowledged, every acknowledgment is preceded by a request, and req*ack* "

... and requests are acknowledged in the order they are received !

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

Class Register Automata

$\mathcal{A}$

$F_{\sim} = \{q_1\}$

$F_{+1} = \{q_1\}$

$G = true$

$\prec_{\sim}$	$\prec_{+1}$	guard	input	target	update
			(req, d)	q_0	$r_1 := d$
	q_0		(req, d)	q_0	$r_1 := d \quad r_2 := (\prec_{+1}, r_1)$
q_0	q_0	$(\prec_{\sim}, r_2) = \bot$	(ack, d)	q_1	$r_1 := d$
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req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state
r_1
r_2

Class Register Automata

$\mathcal{A}$

$F_\sim = \{q_1\}$

$F_{+1} = \{q_1\}$

$G = true$

$\prec_\sim$	$\prec_{+1}$	guard	input	target	update
			(req, d)	q_0	$r_1 := d$
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req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0
r_1	8
r_2	$\perp$

Class Register Automata

$\mathcal{A}$

$F_\sim = \{q_1\}$

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$G = true$

$\prec_\sim$	$\prec_{+1}$	guard	input	target	update
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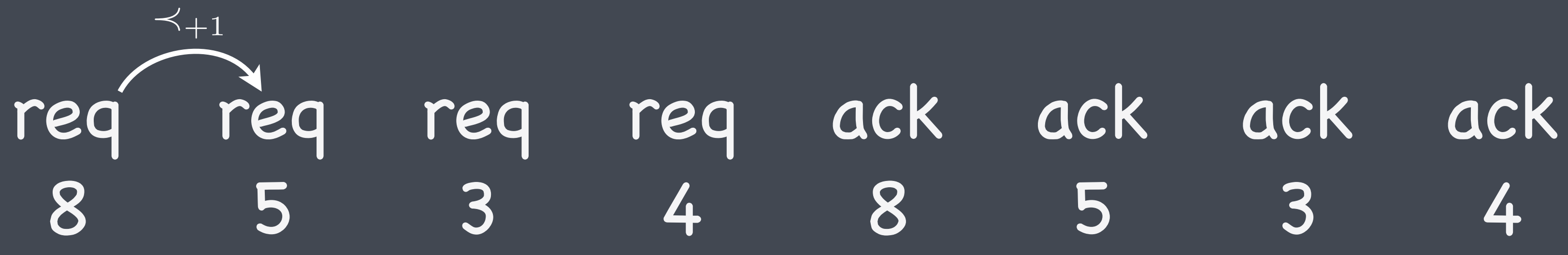

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0	q_0
r_1	8	5
r_2	$\perp$	8

Class Register Automata

$\mathcal{A}$

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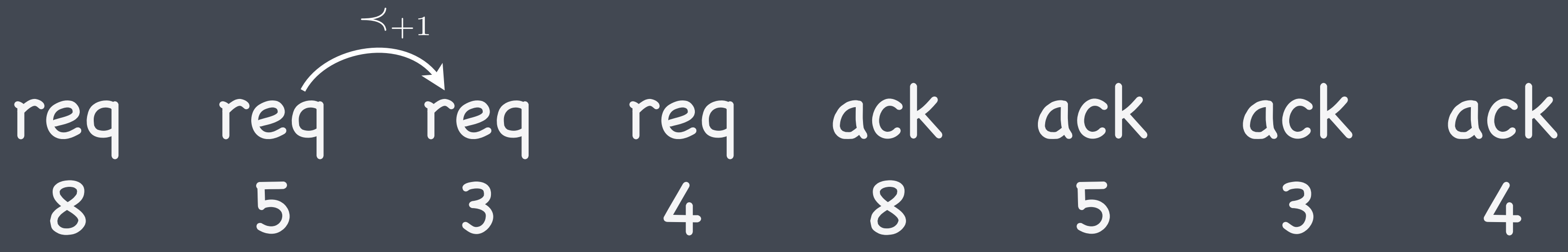

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0	q_0	q_0
r_1	8	5	3
r_2	$\bot$	8	5

Class Register Automata

$\mathcal{A}$

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$F_{+1} = \{q_1\}$

$G = true$

$\prec_{\sim}$	$\prec_{+1}$	guard	input	target	update
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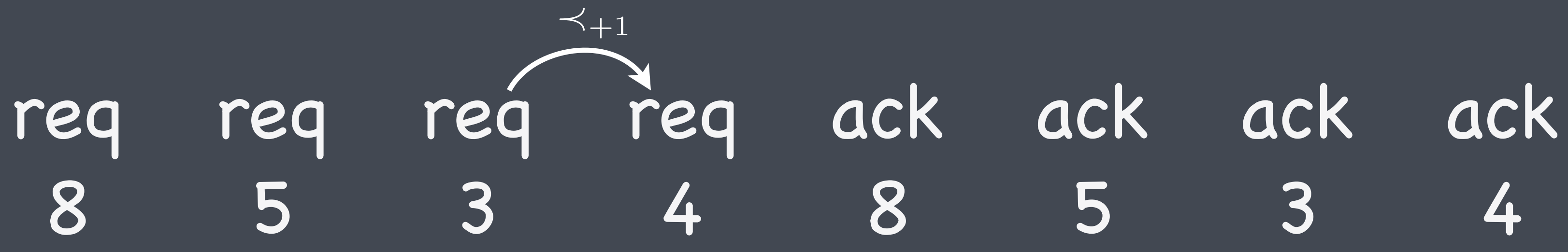

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0	q_0	q_0	q_0
r_1	8	5	3	4
r_2	$\perp$	8	5	3

Class Register Automata

$\mathcal{A}$

$\prec_\sim$	$\prec_{+1}$	guard	input	target	update
			(req, d)	q_0	$r_1 := d$
	q_0		(req, d)	q_0	$r_1 := d \quad r_2 := (\prec_{+1}, r_1)$
q_0	q_0	$(\prec_\sim, r_2) = \bot$	(ack, d)	q_1	$r_1 := d$
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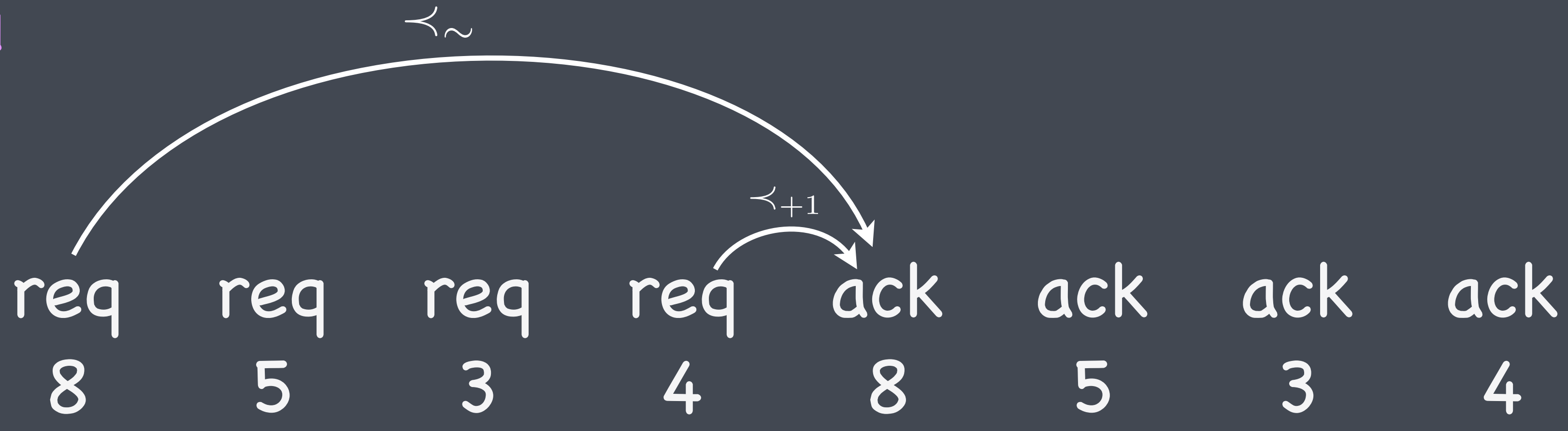

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0	q_0	q_0	q_0	q_1
r_1	8	5	3	4	8
r_2	$\bot$	8	5	3	$\bot$

Class Register Automata

$\mathcal{A}$

$F_\sim = \{q_1\}$

$F_{+1} = \{q_1\}$

$G = true$

$\prec_\sim$	$\prec_{+1}$	guard	input	target	update
			(req, d)	q_0	$r_1 := d$
	q_0		(req, d)	q_0	$r_1 := d$ $\quad r_2 := (\prec_{+1}, r_1)$
q_0	q_0	$(\prec_\sim, r_2) = \bot$	(ack, d)	q_1	$r_1 := d$
q_0	q_1	$(\prec_\sim, r_2) = (\prec_{+1}, r_1)$	(ack, d)	q_1	$r_1 := d$

$L(\mathcal{A}) =$ " every process sends one request, which is acknowledged, every acknowledgment is preceded by a request, and req*ack* "

... and requests are acknowledged in the order they are received !

req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

state	q_0	q_0	q_0	q_0	q_1	q_1
r_1	8	5	3	4	8	5
r_2	$\bot$	8	5	3	$\bot$	$\bot$

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	q_0		(req, d)	q_0	$r_1 := d \quad r_2 := (\prec_{+1}, r_1)$
q_0	q_0	$(\prec_\sim, r_2) = \perp$	(ack, d)	q_1	$r_1 := d$
q_0	q_1	$(\prec_\sim, r_2) = (\prec_{+1}, r_1)$	(ack, d)	q_1	$r_1 := d$

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req	req	req	req	ack	ack	ack	ack
8	5	3	4	8	5	3	4

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r_1	8	5	3	4	8	5	3	4
r_2	$\perp$	8	5	3	$\perp$	$\perp$	$\perp$	$\perp$

From Logic to Automata

From Logic to Automata

- EMSO$^2(\prec_\sim, \prec_{+1}, <, \prec_\sim^*)$ = class memory automata
  [Bojanczyk, David, Muscholl, Schwentick, Segoufin 2006]
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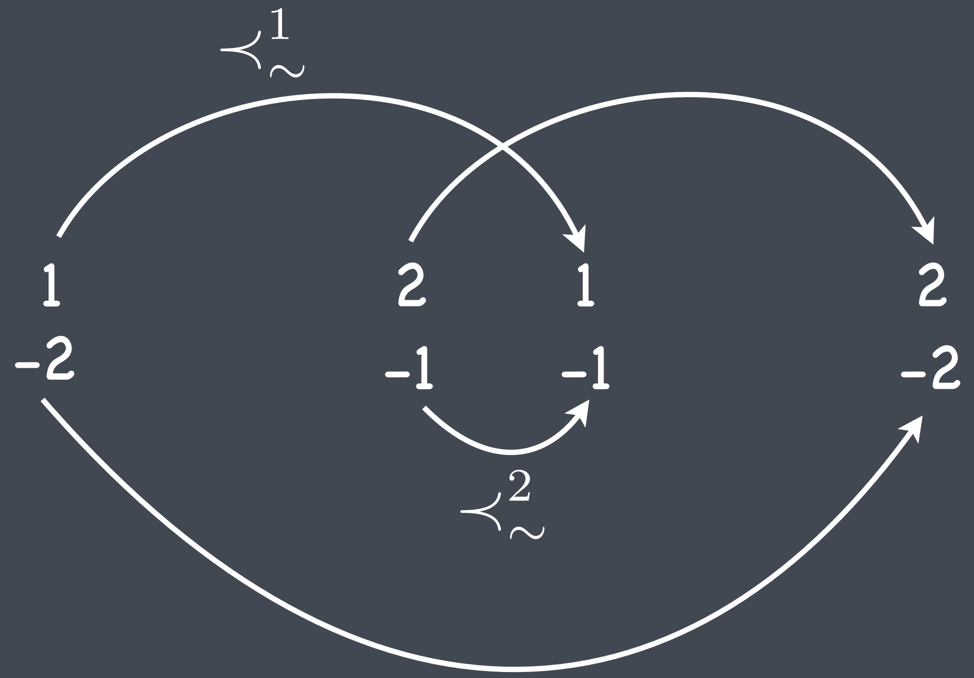

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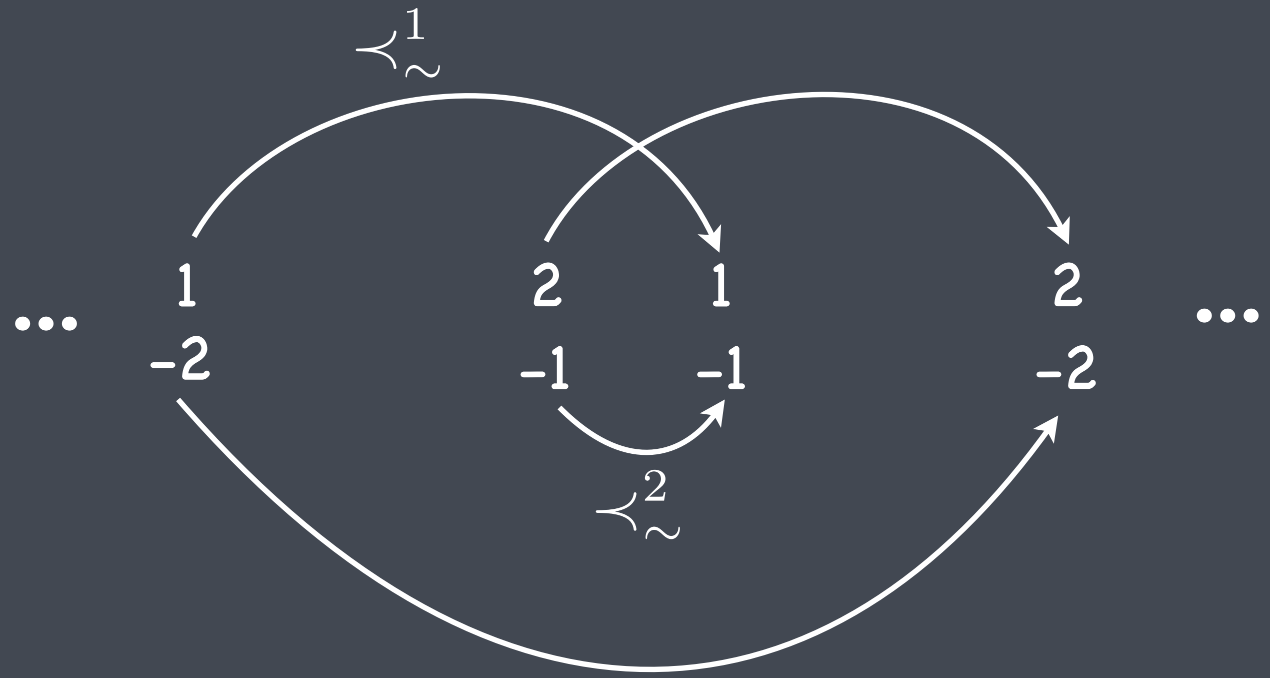

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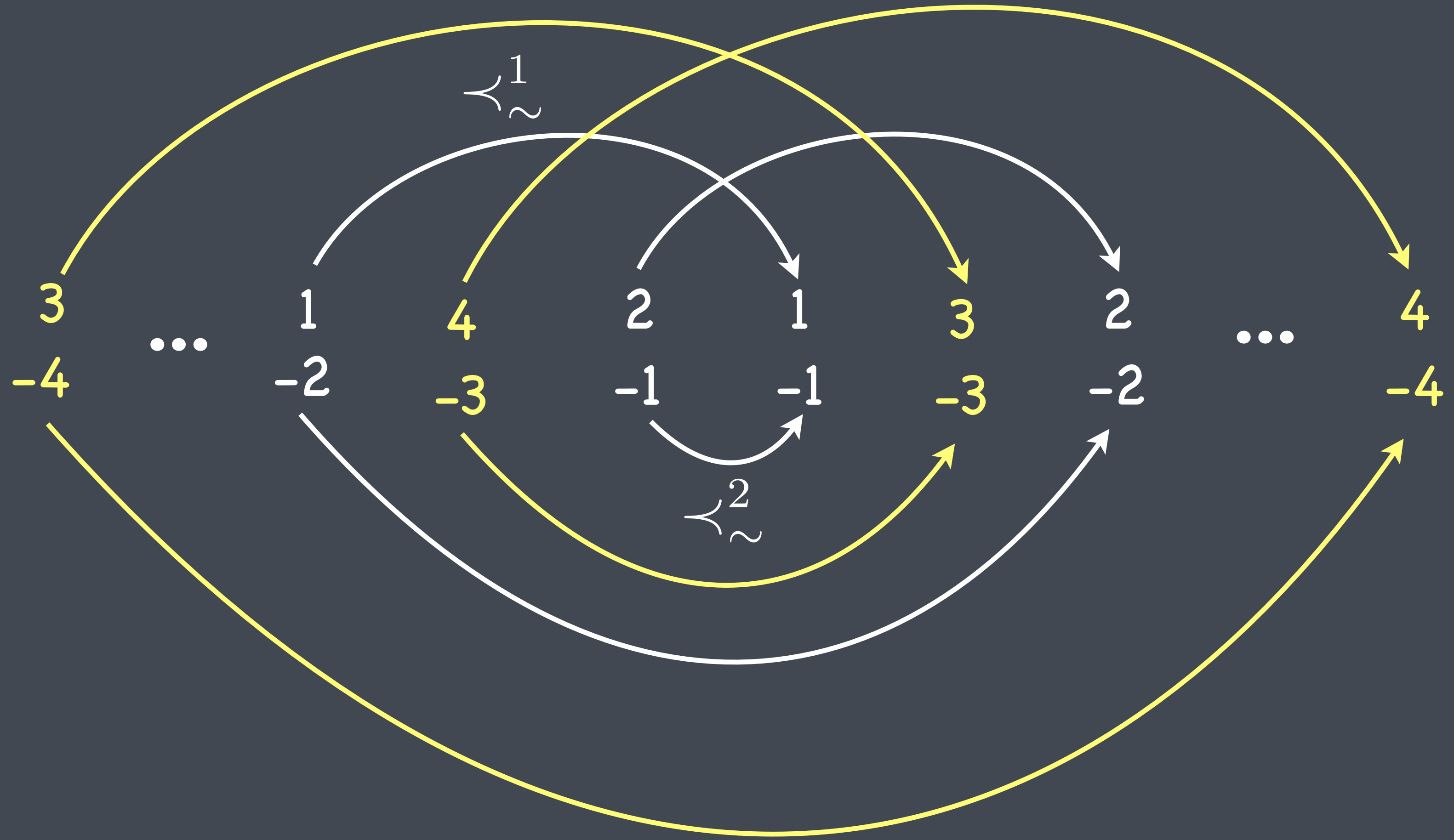

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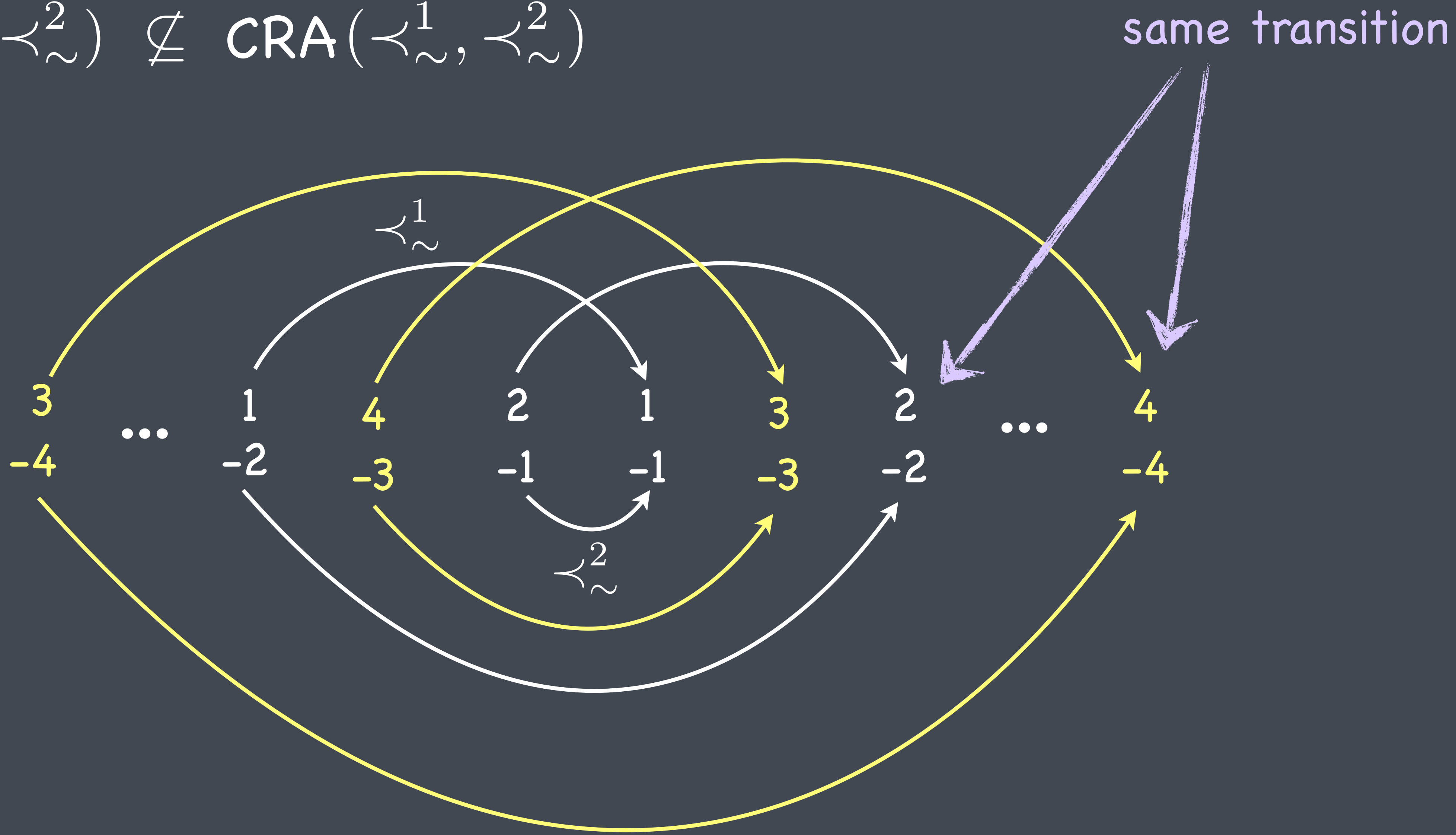

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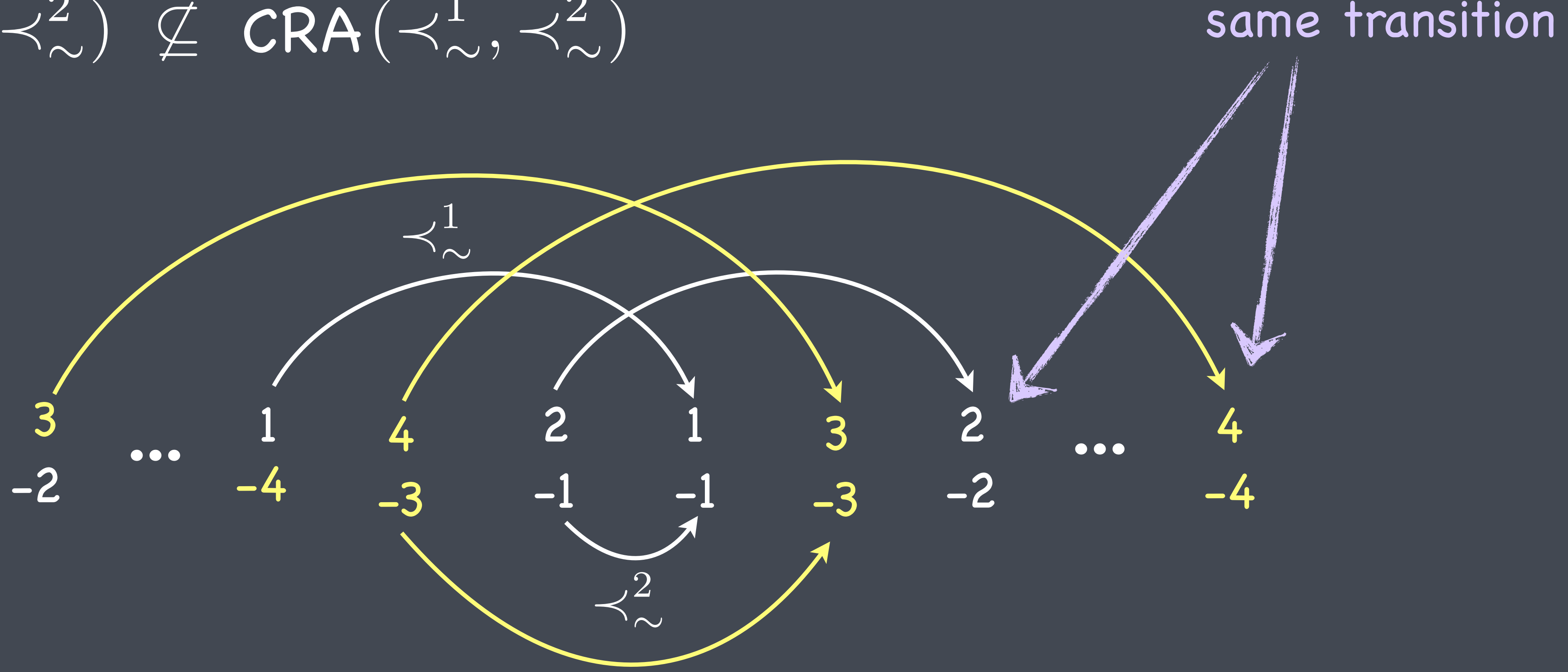

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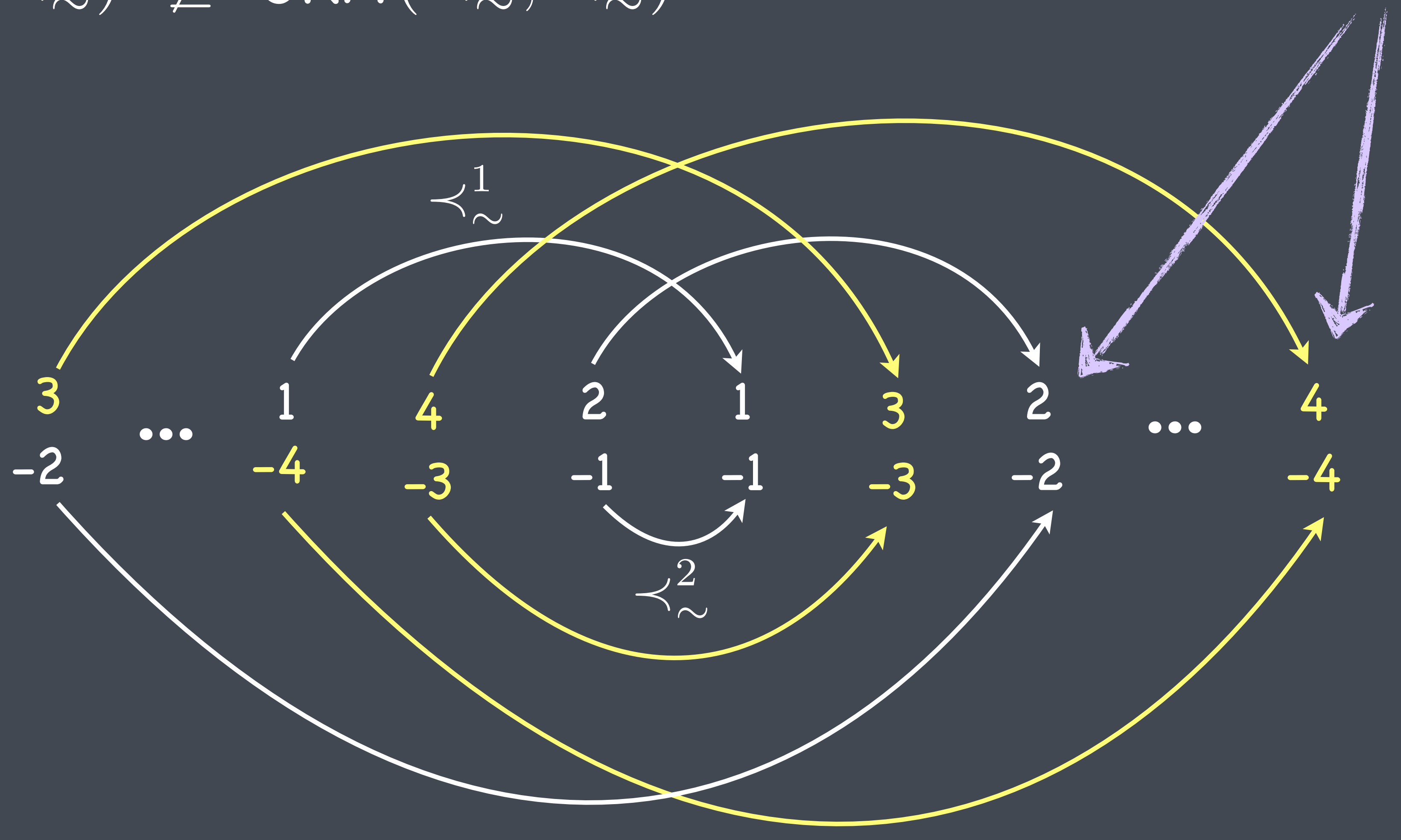
same transition



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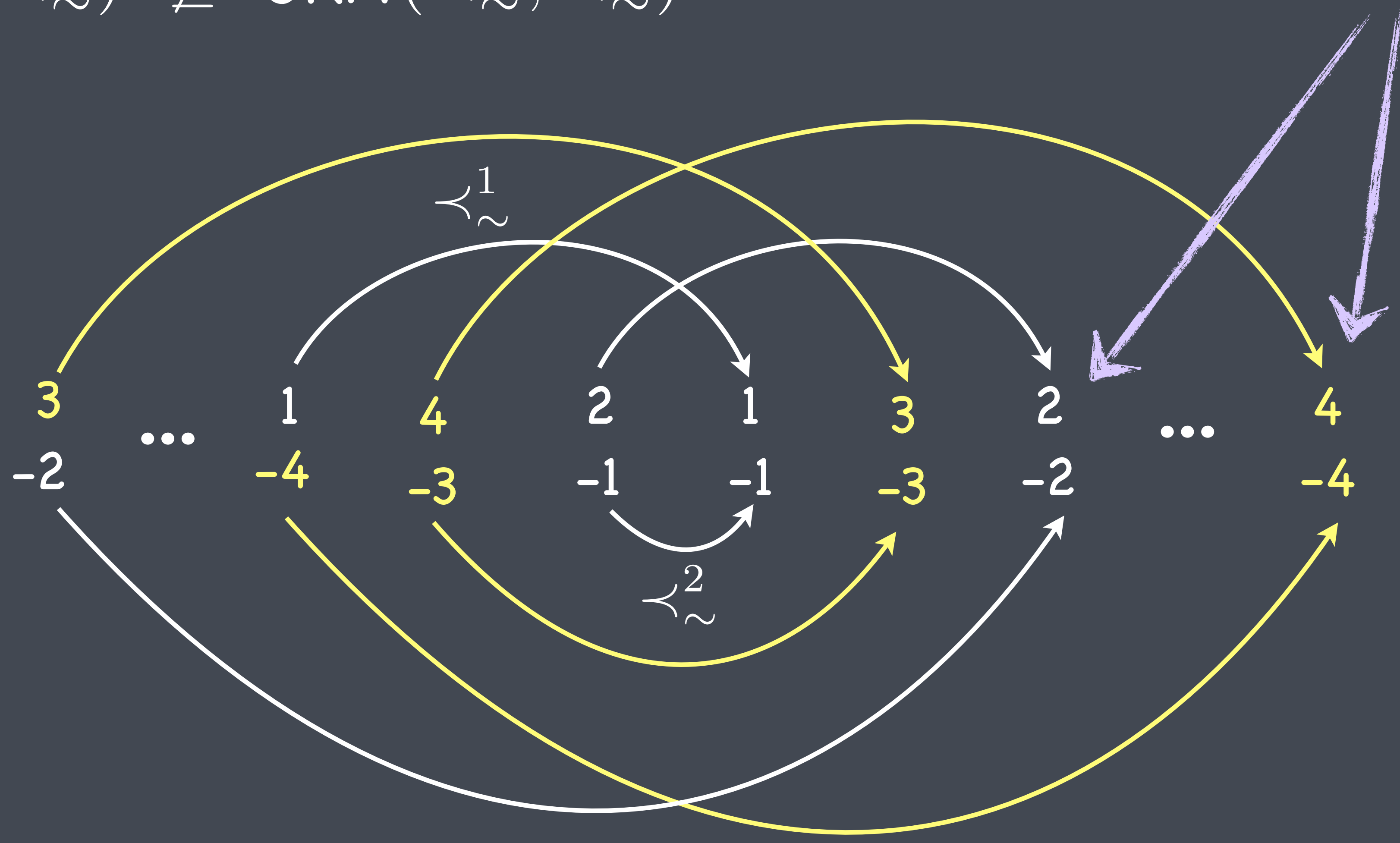

same transition

=> CRA cannot detect cycles

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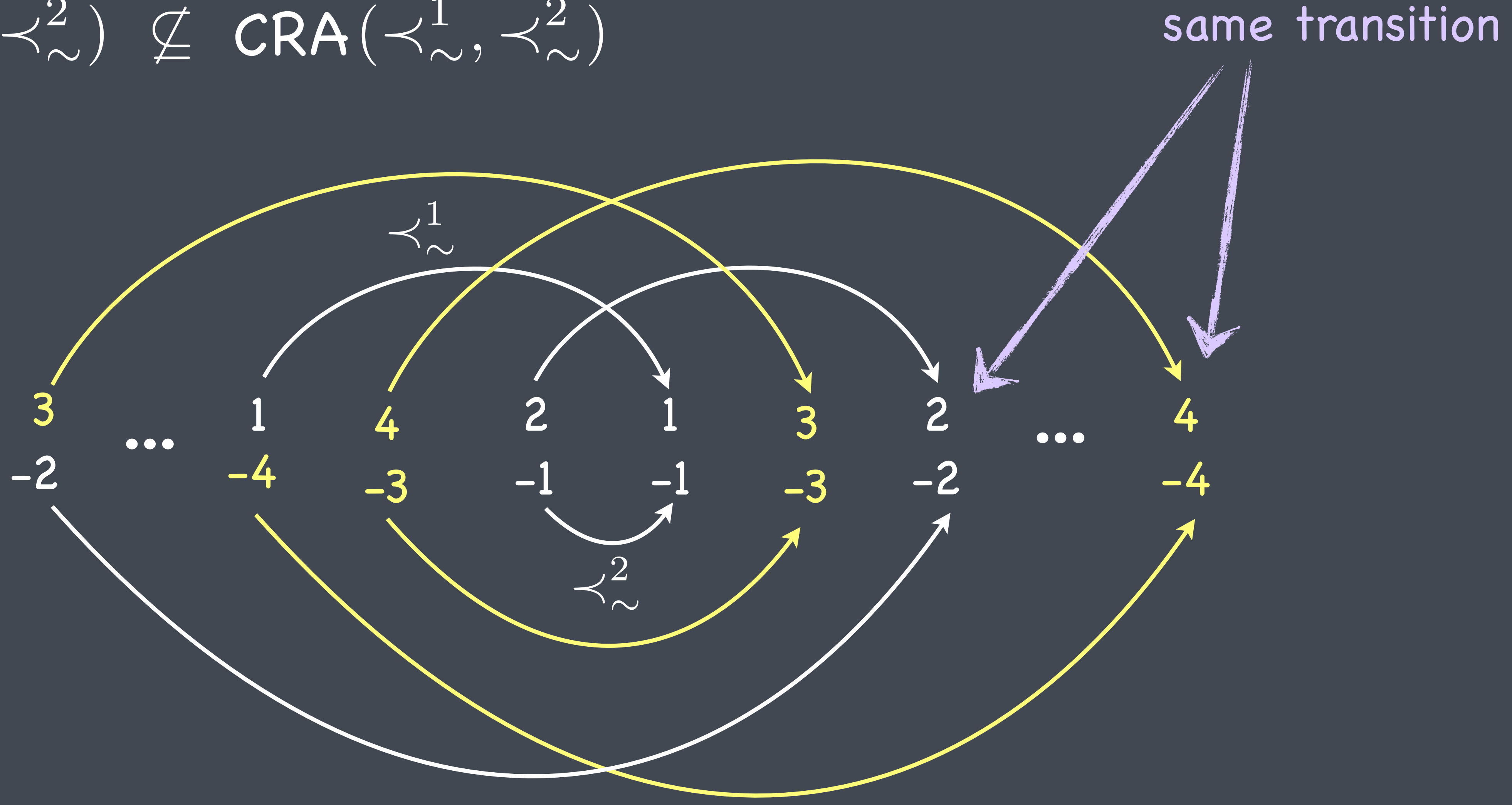


=> CRA cannot detect cycles

=> guess data values!

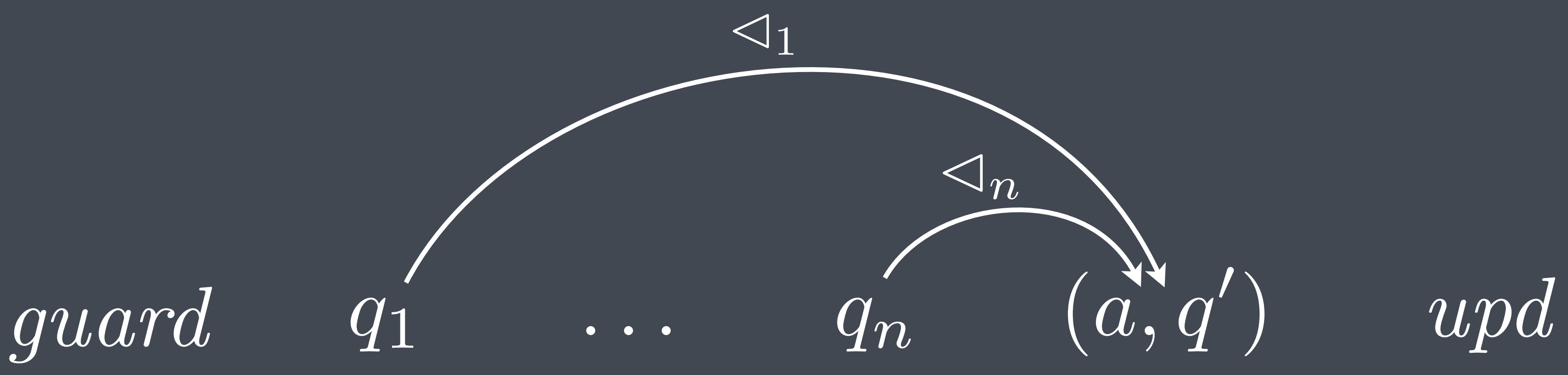
Class Register Automata (with guess)

over S = $\{\lhd_1, \ldots, \lhd_n\}$

$$\mathcal{A} = (Q, R, \longrightarrow, F, G)$$

- Q finite set of states
- R finite set of registers
- transition relation:

- $F = (F_{\lhd_1}, \ldots, F_{\lhd_n})$
- $G \in \mathcal{B}(\text{“}q \leq N\text{”})$



$upd : R \rightharpoonup ((S \times R) \cup \{1, \ldots, m\})$

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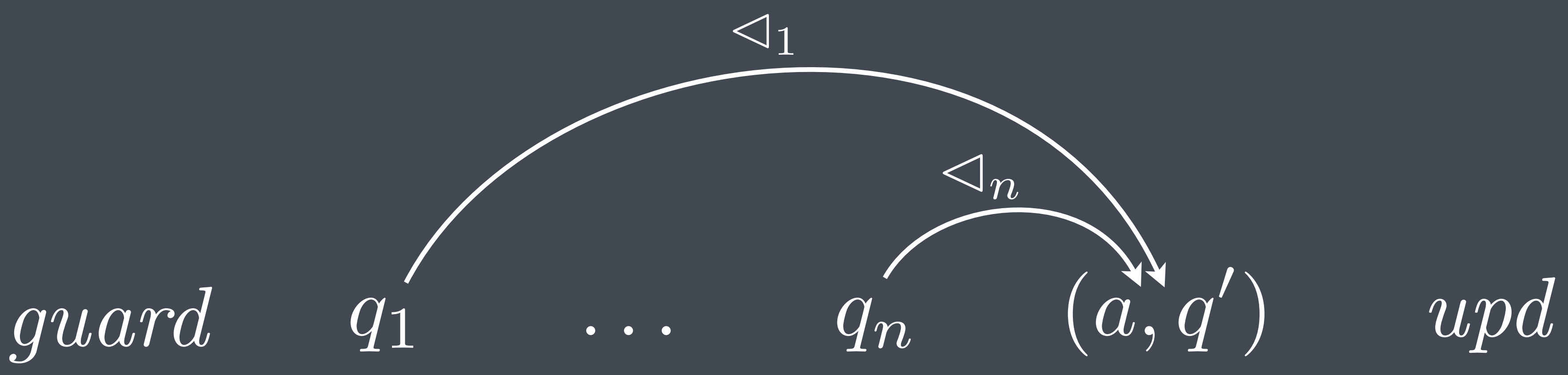

$upd : R \rightharpoonup ((S \times R) \cup \{1, \dots, m\})$

$\cup$ {guess}

- $F = (F_{\lhd_1}, \dots, F_{\lhd_n})$
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guessing register automata:
[Kaminski, Zeitlin 2010]

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Theorem: For every signature S, EMSO(S) $\subseteq$ ${}_{g}$CRA(S).

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Proof:

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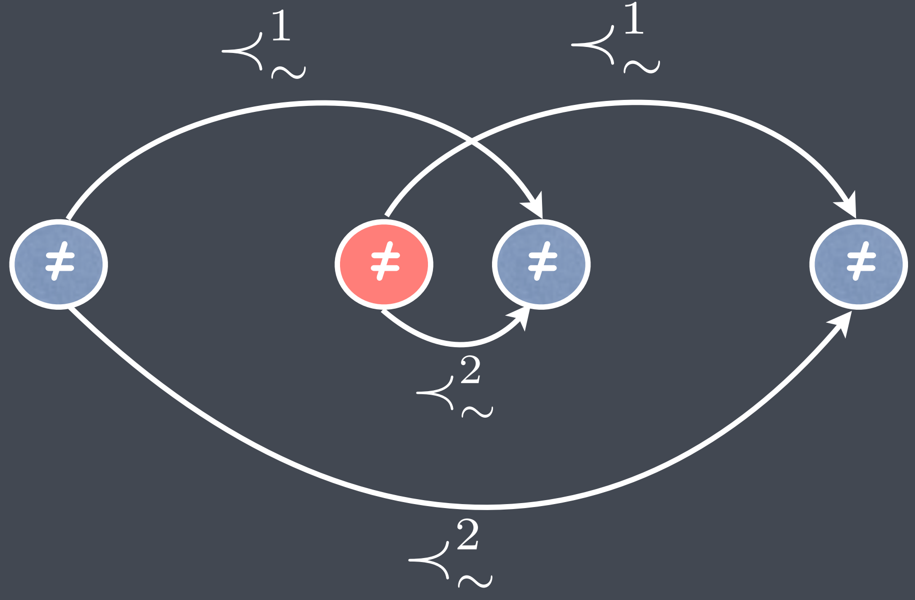

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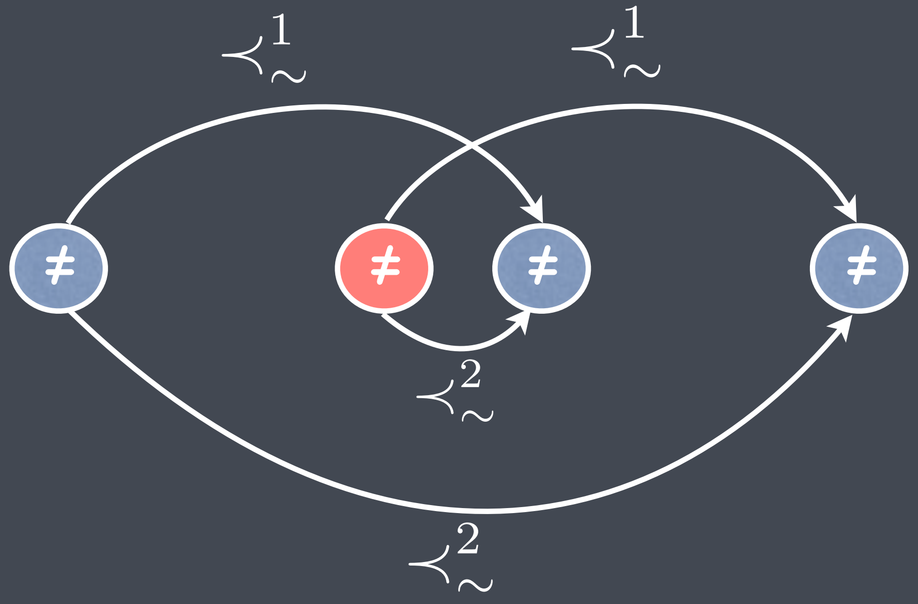
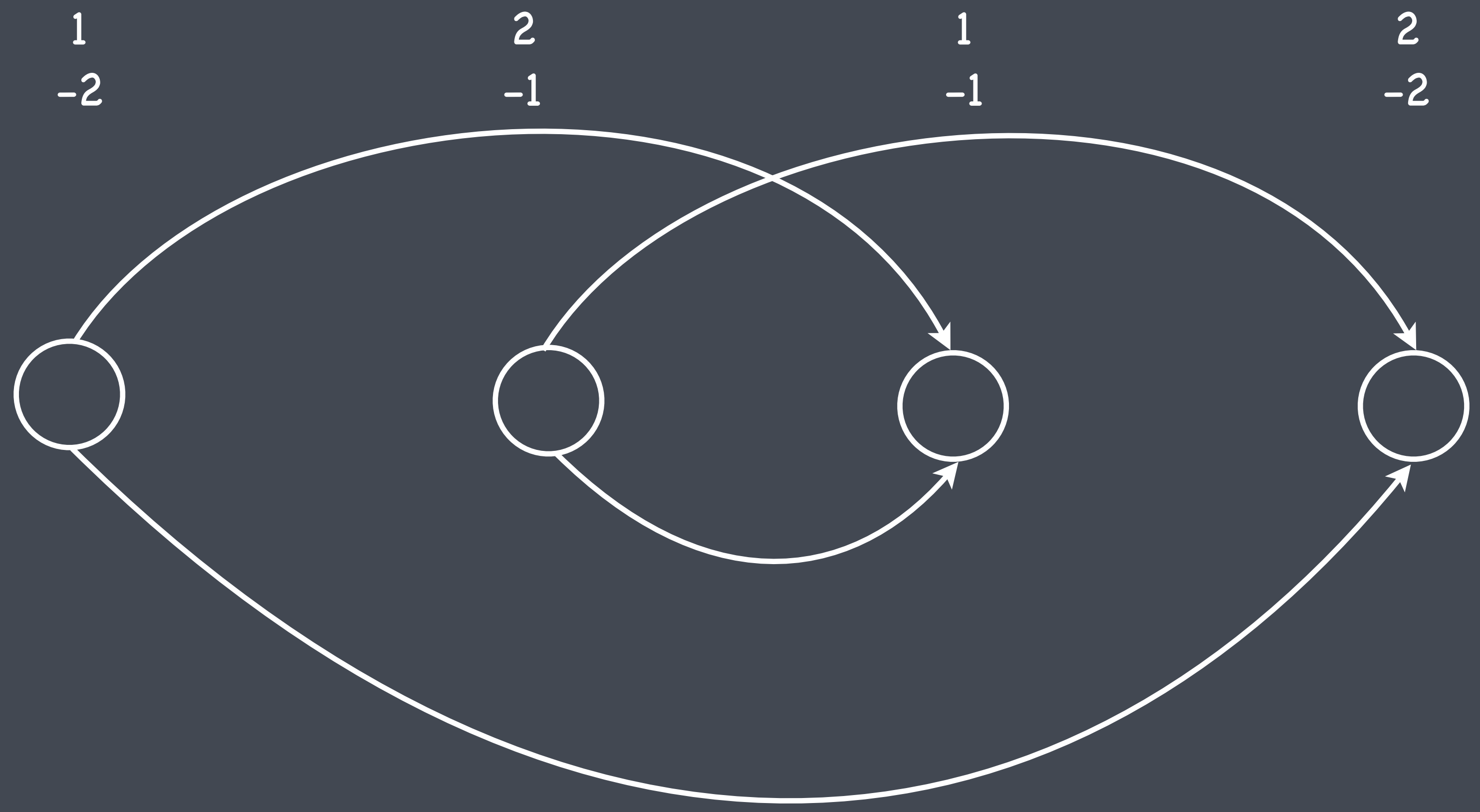


- => Build class register automaton that detects spheres

Sphere Automaton



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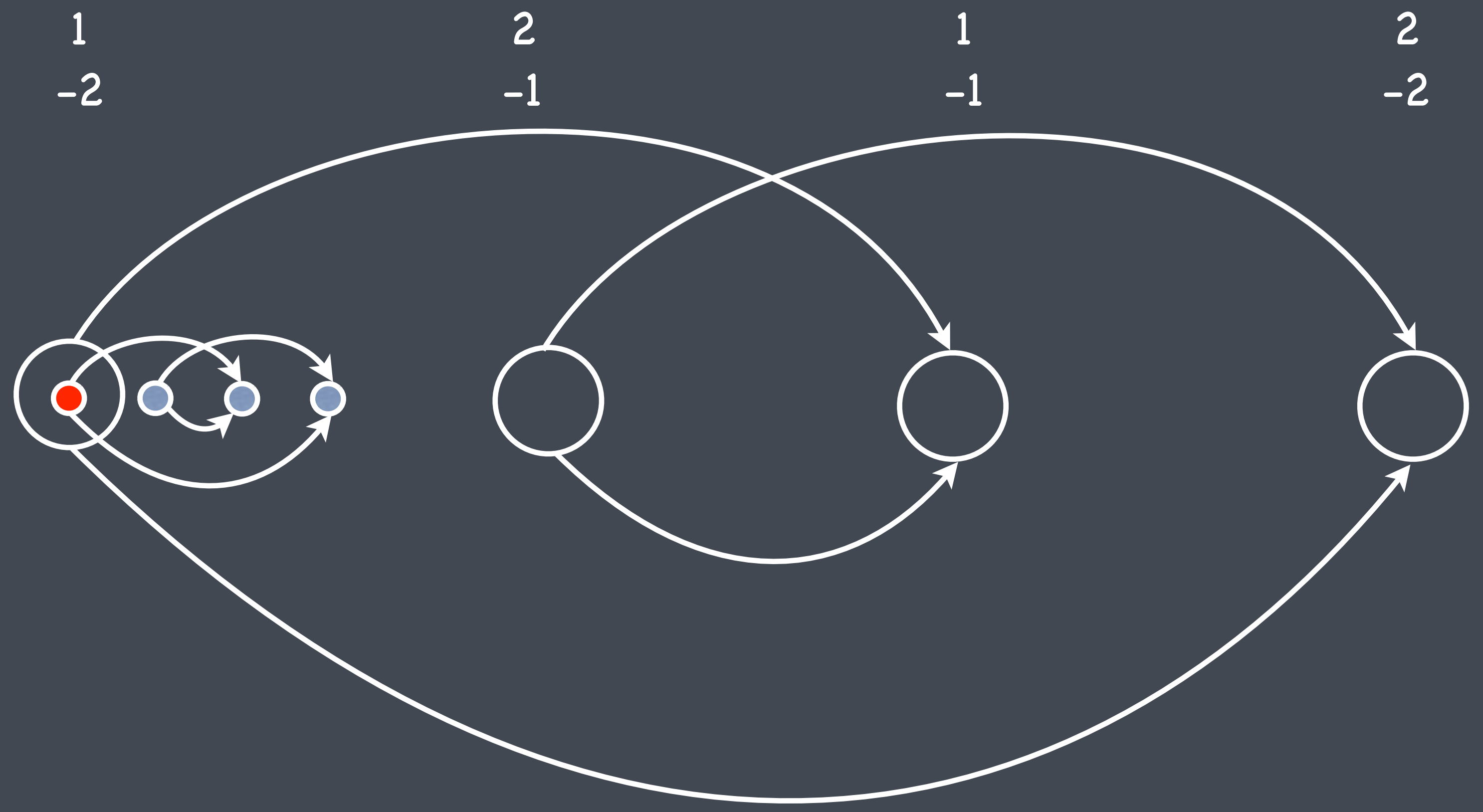

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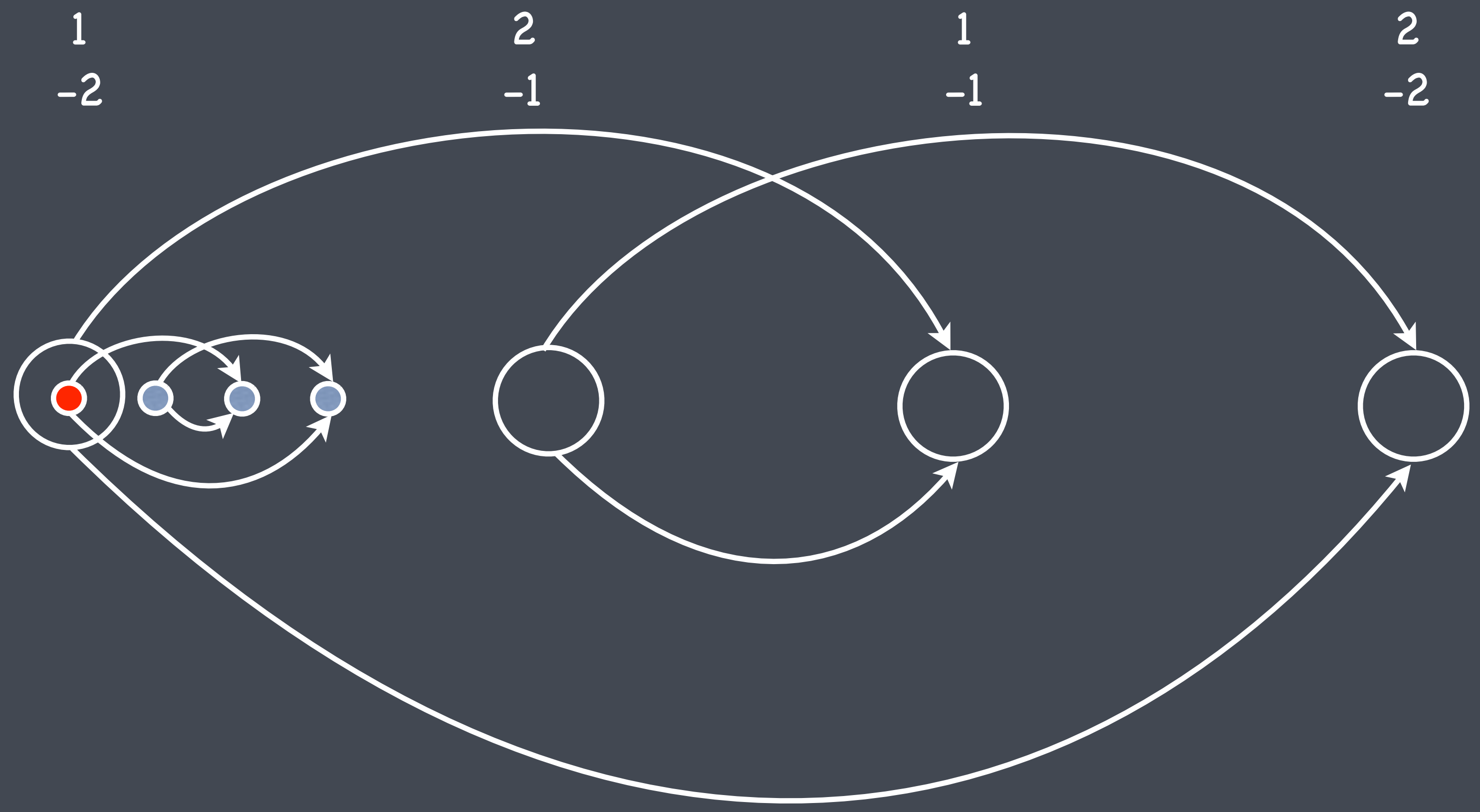
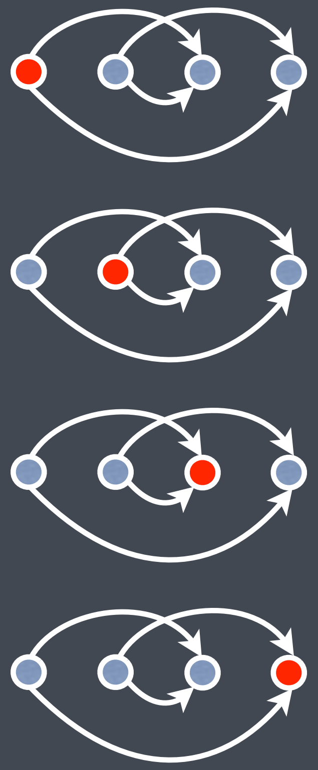


Registers:



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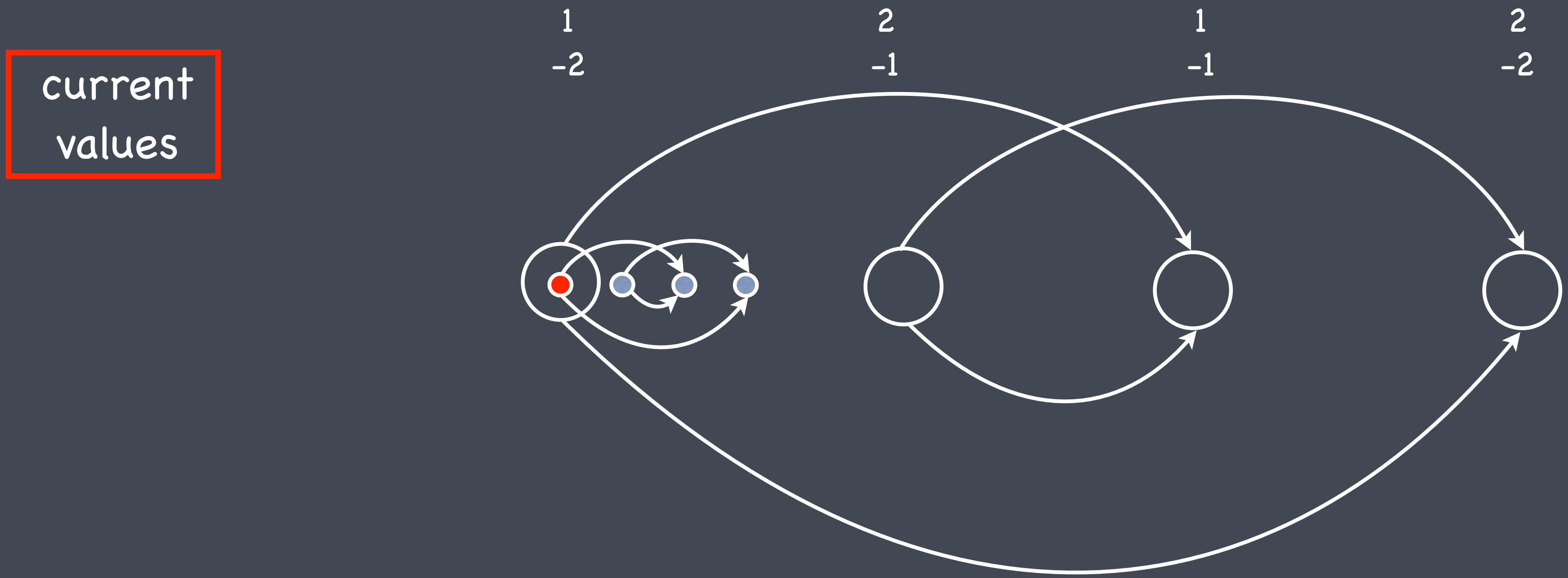

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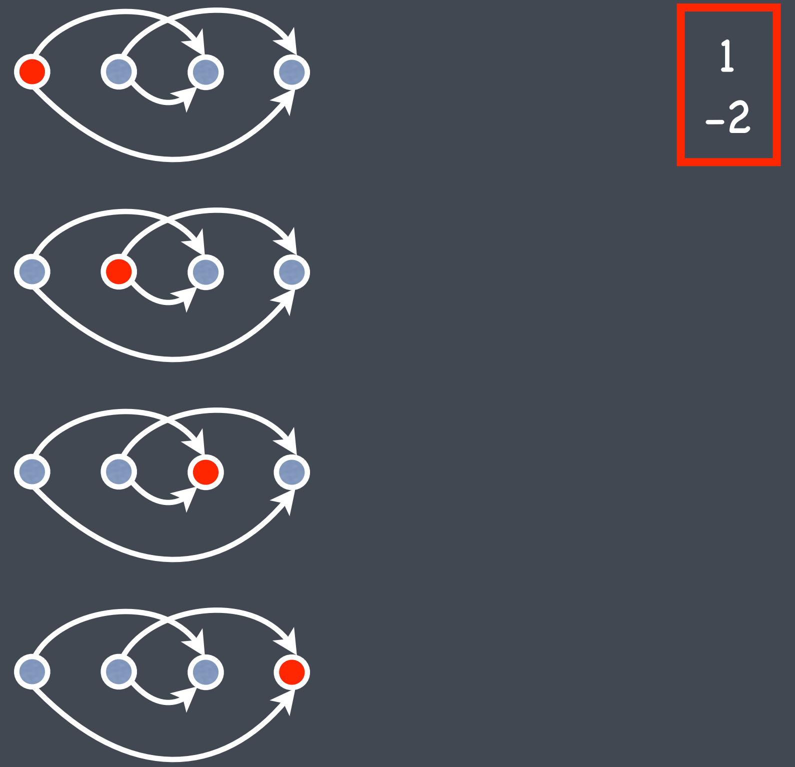
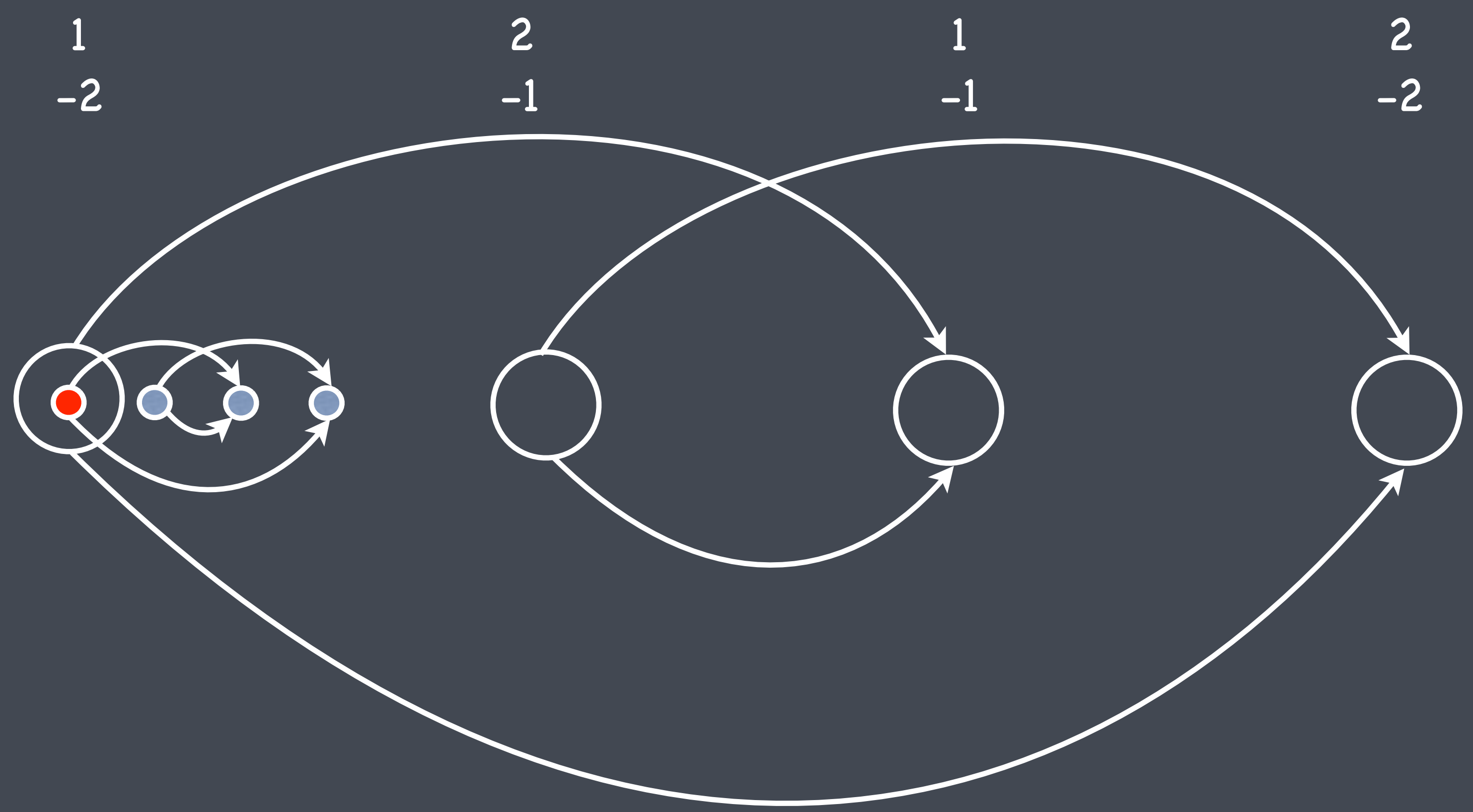


Sphere Automaton

current values

guessed values



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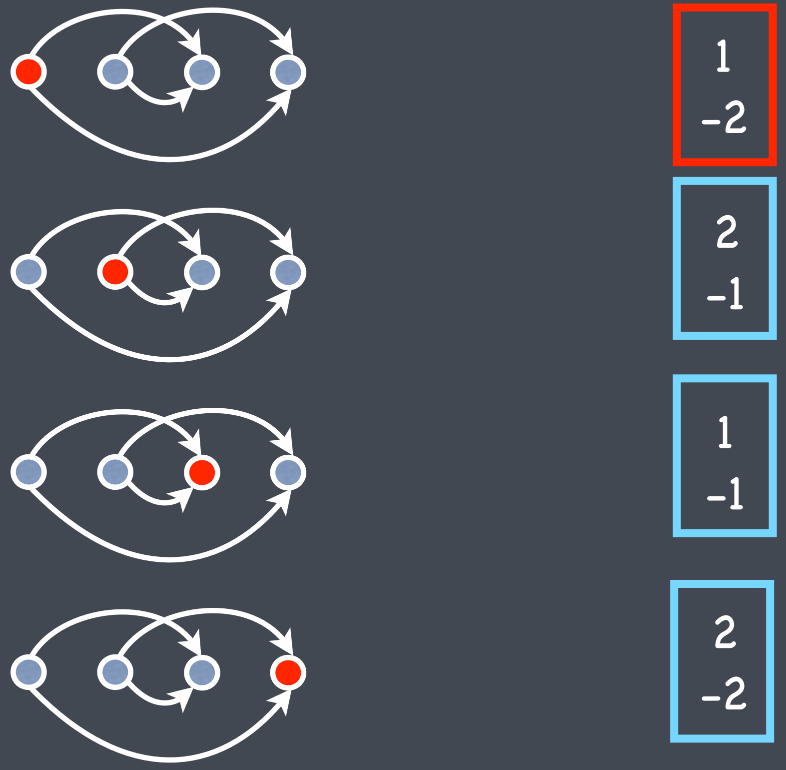

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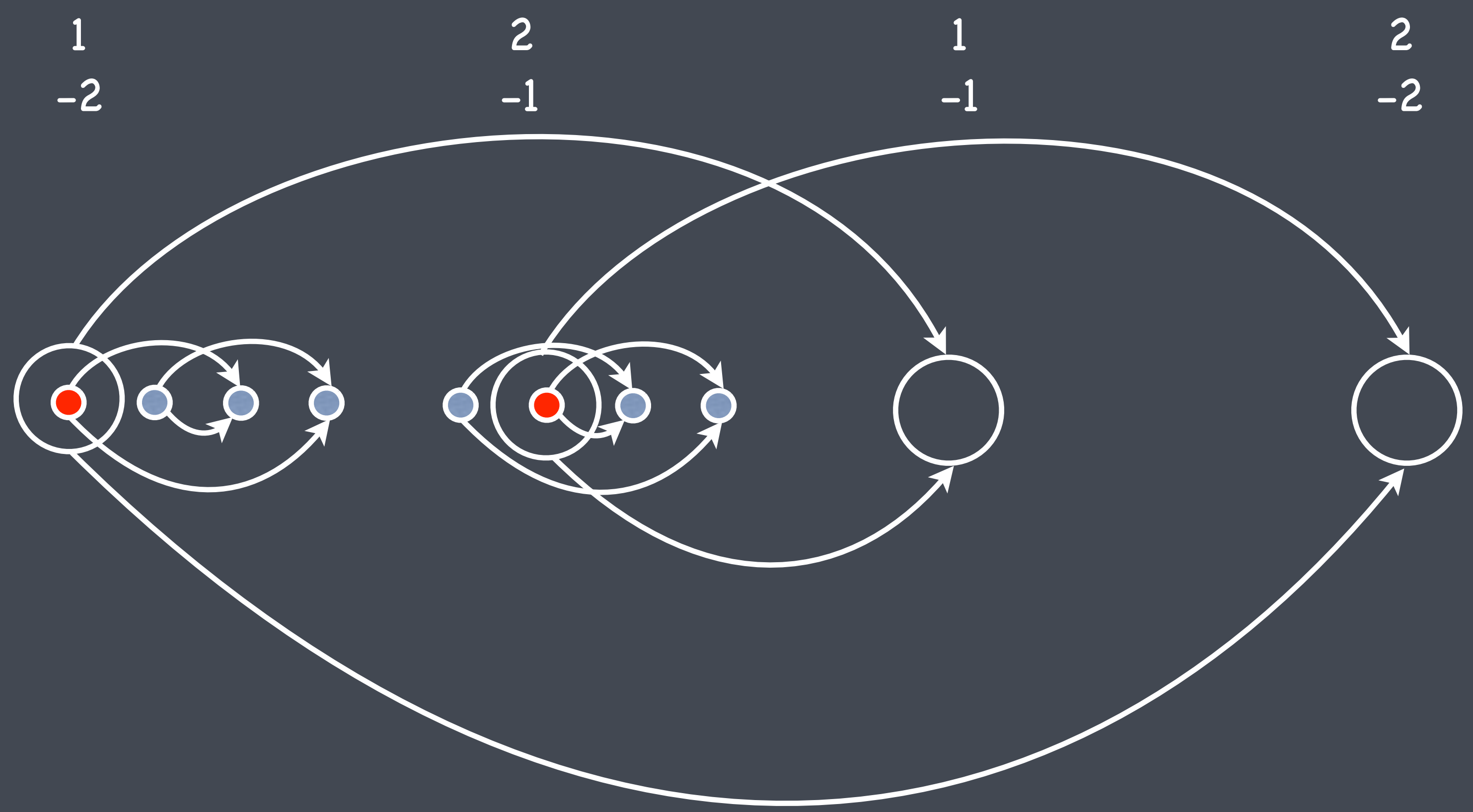

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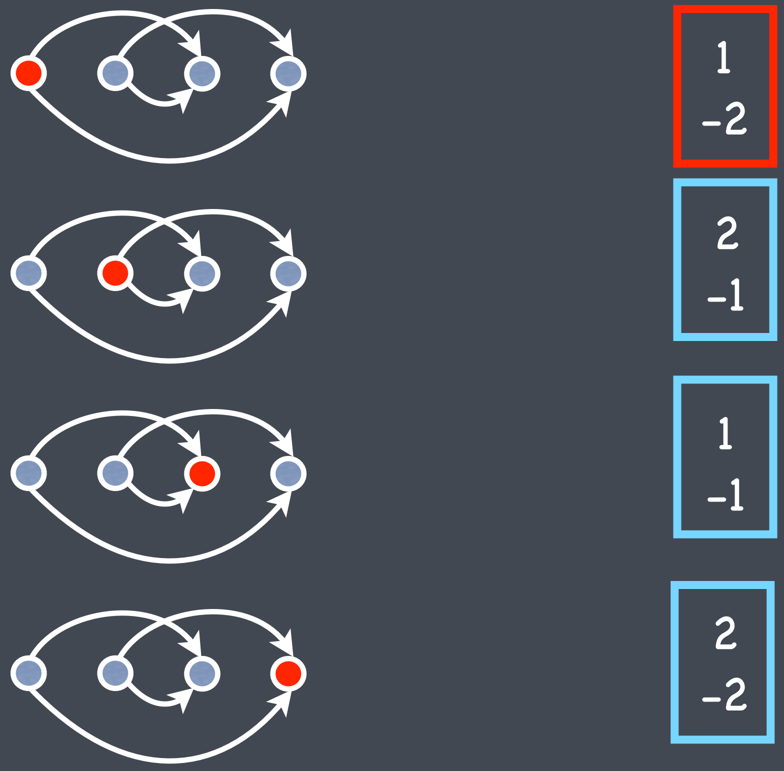

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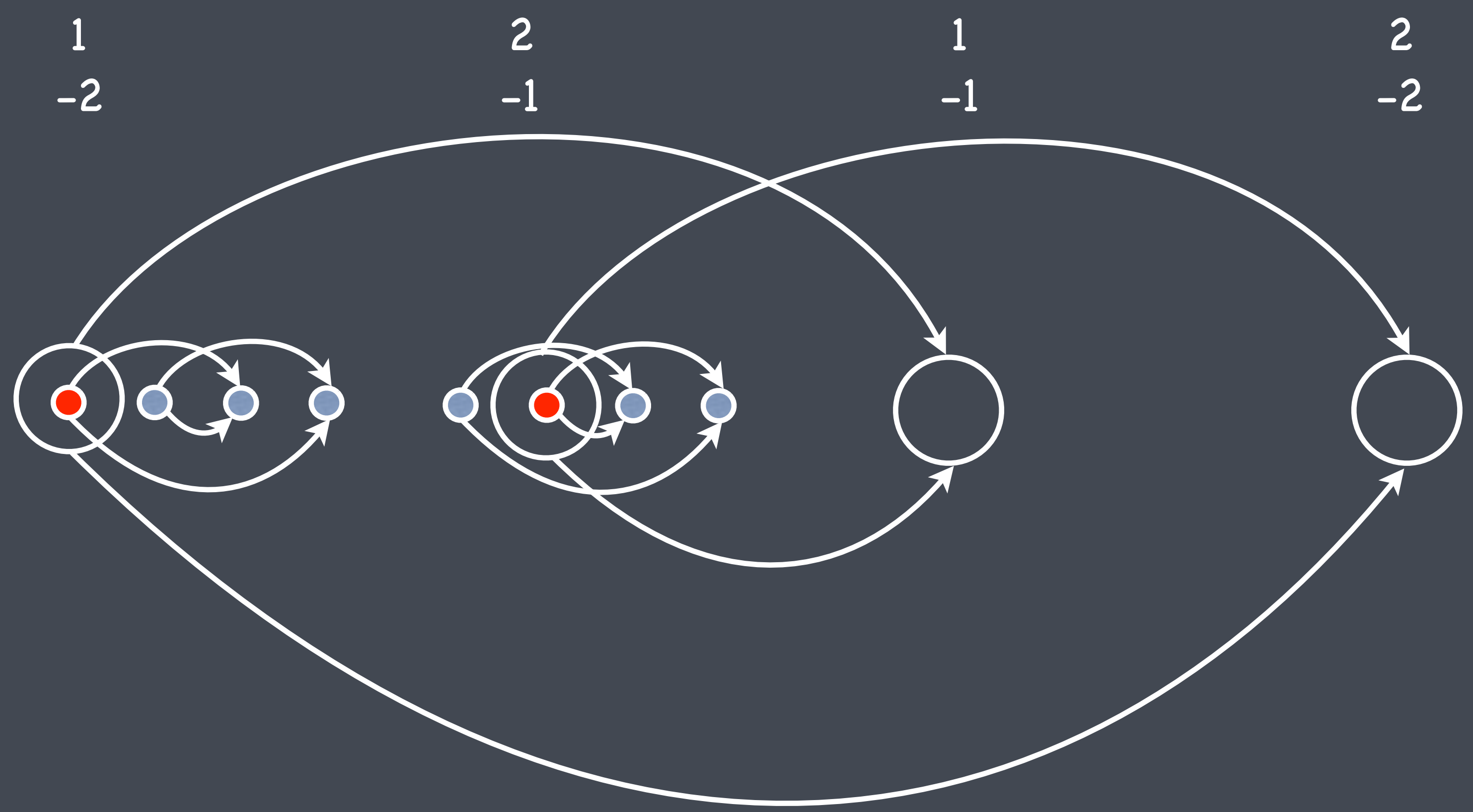

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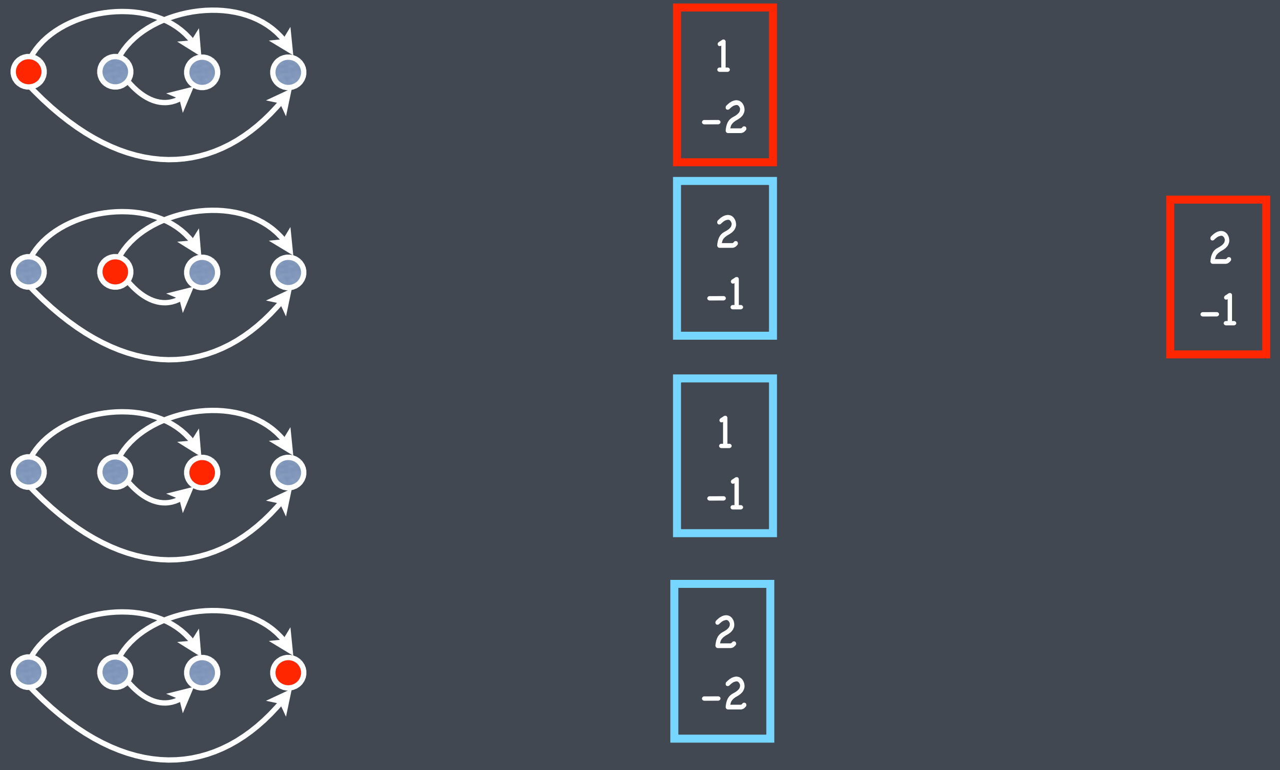

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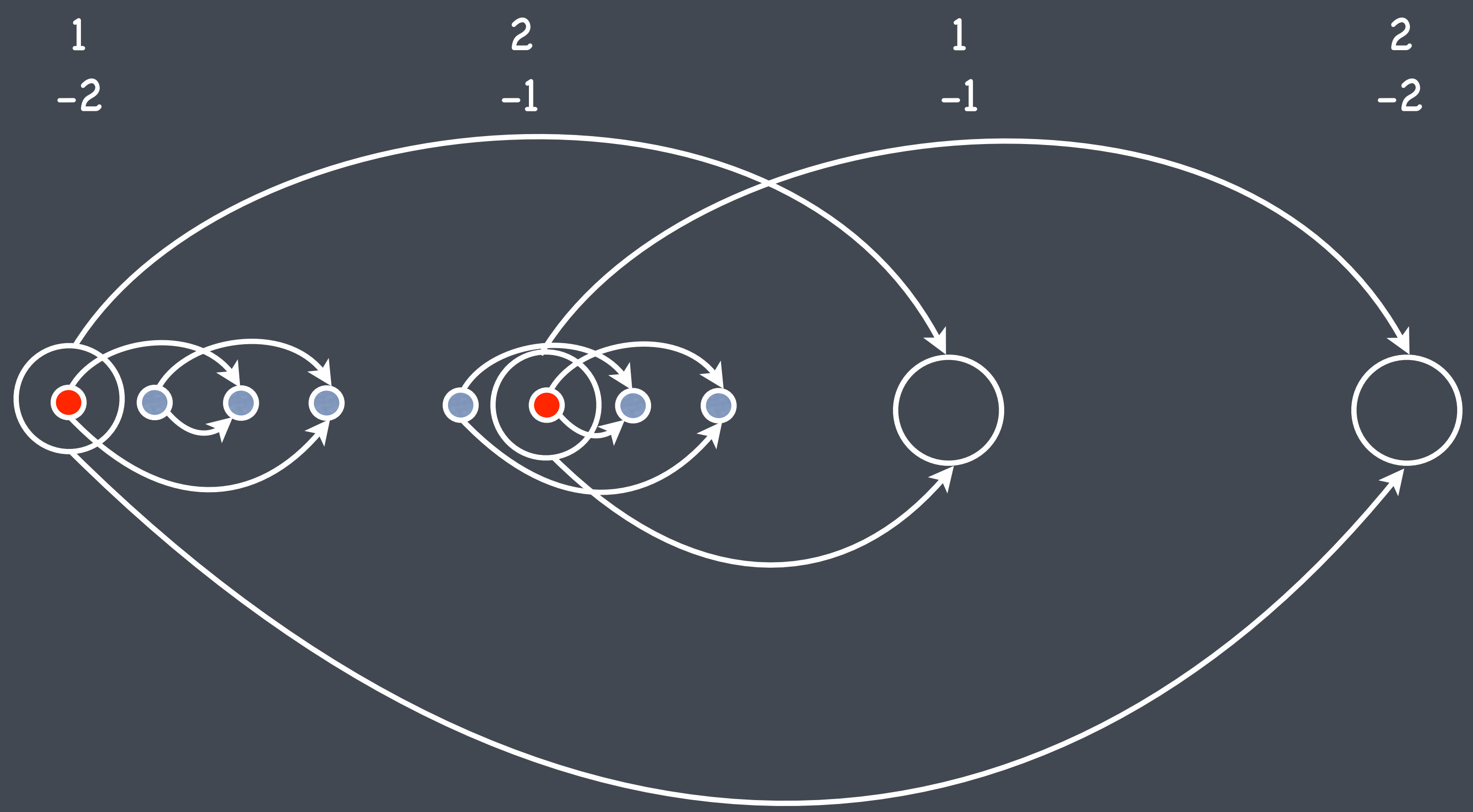

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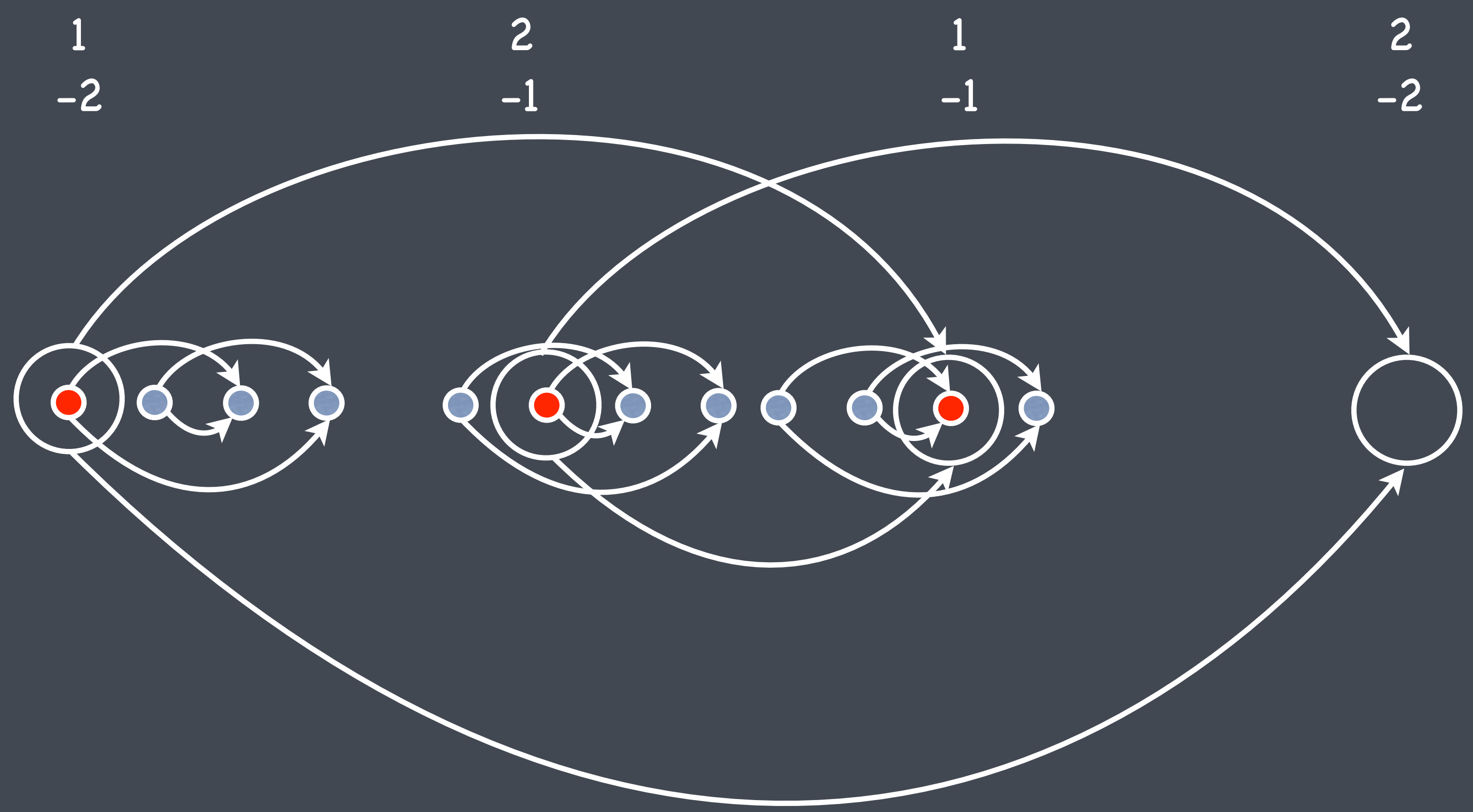

Registers:

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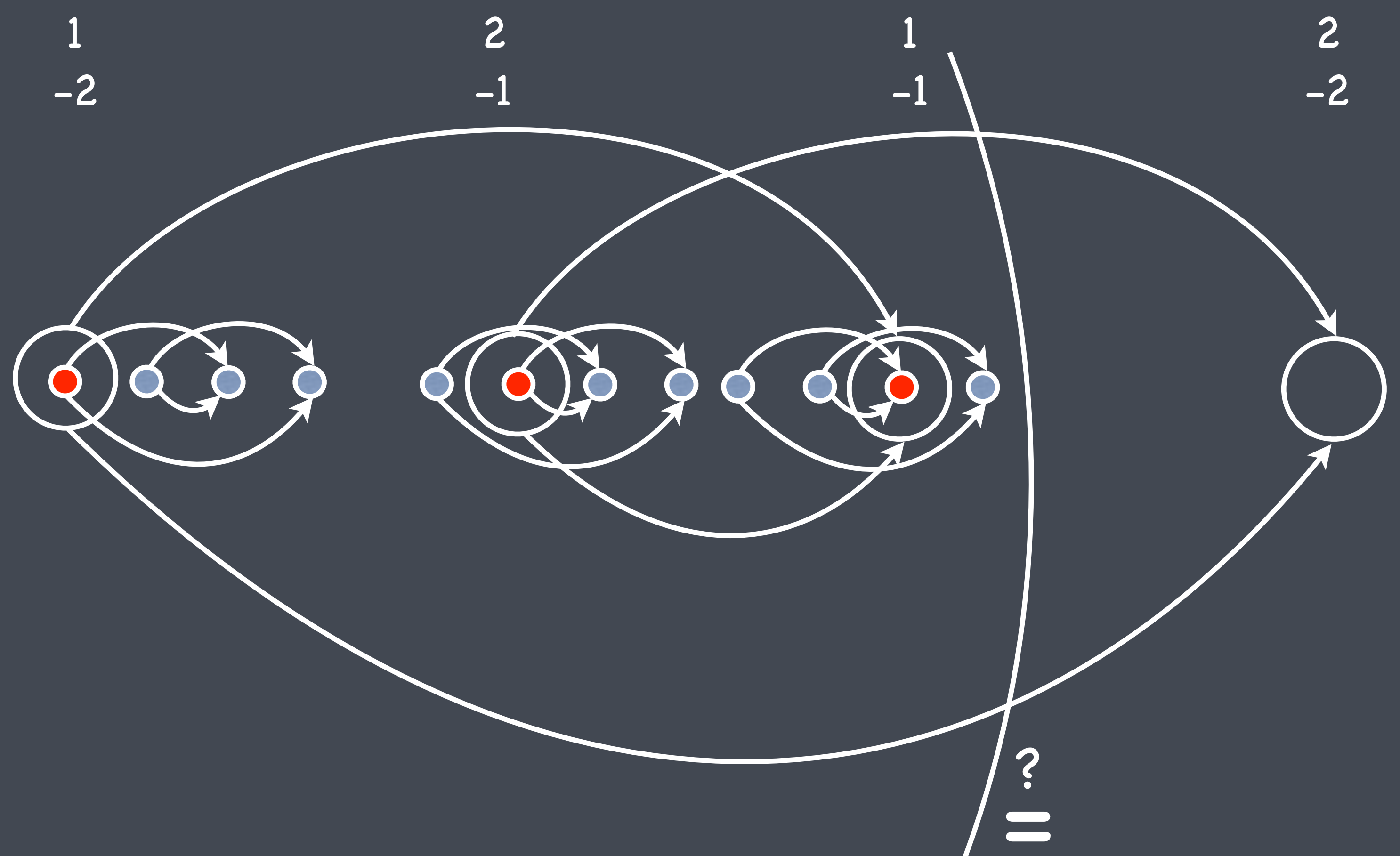
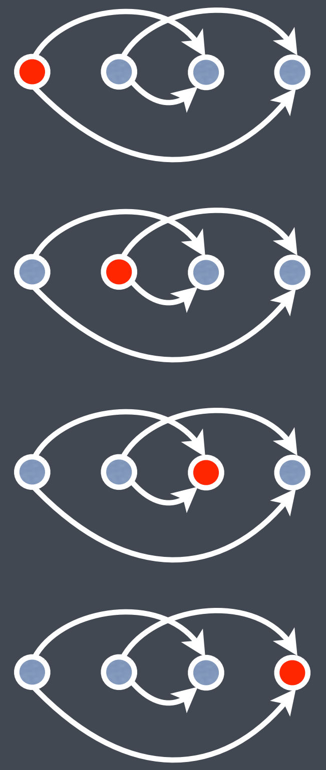


Registers:



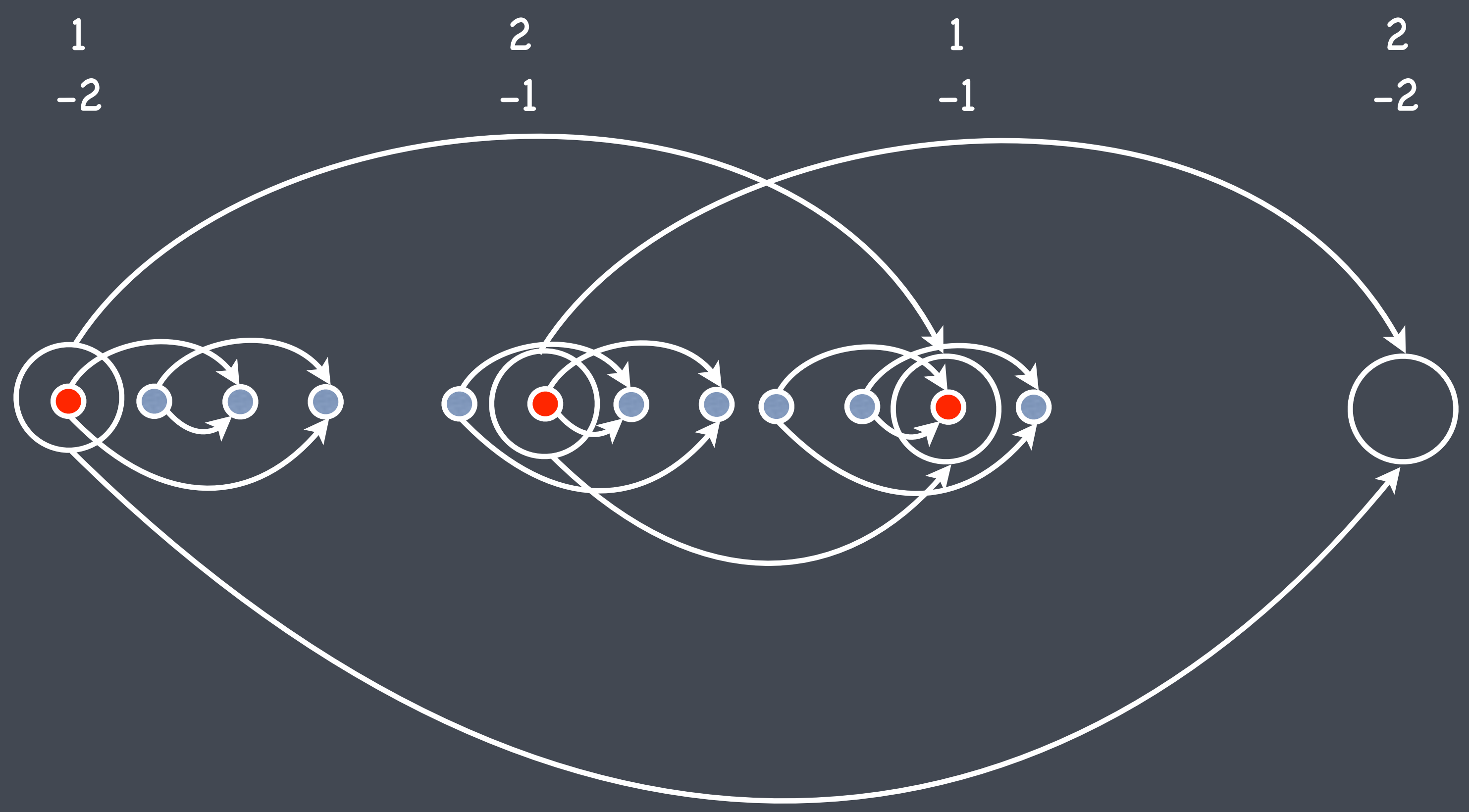
1 -2	$\overset{?}{=}$	1 -2
2 -1	$\overset{?}{=}$	2 -1
1 -1	$\overset{?}{=}$	1 -1
2 -2	$\overset{?}{=}$	2 -2

Sphere Automaton

current values

guessed values

previous values



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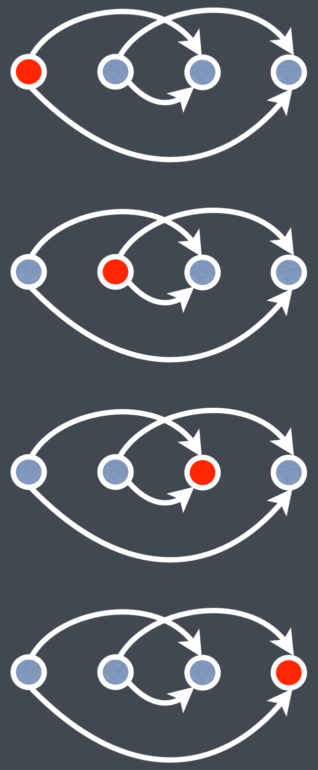


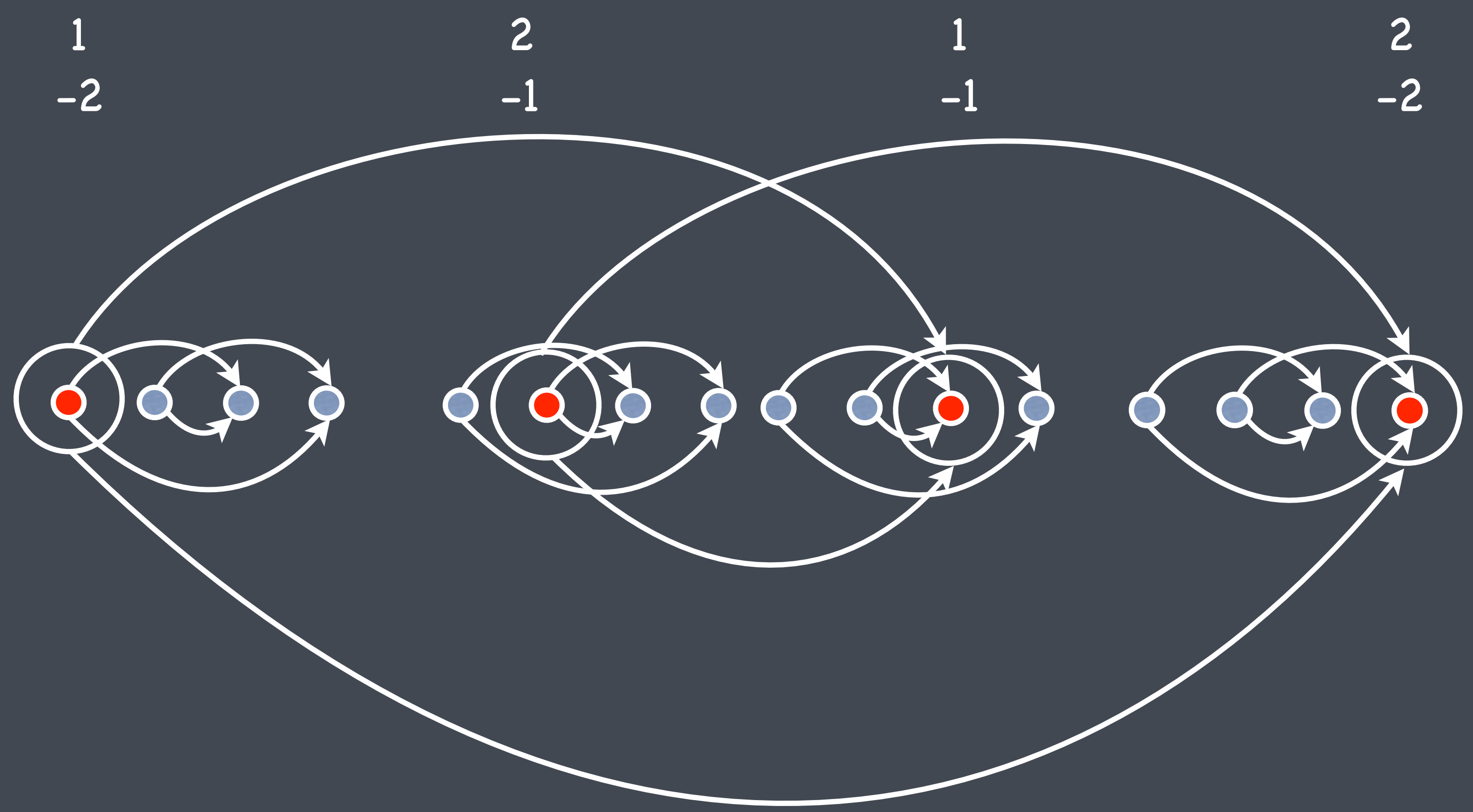
1 -2	1 -2	update →	1 -2
2 -1	2 -1	update →	2 -1
1 -1	1 -1	update →	1 -1
2 -2	2 -2	update →	2 -2

Sphere Automaton

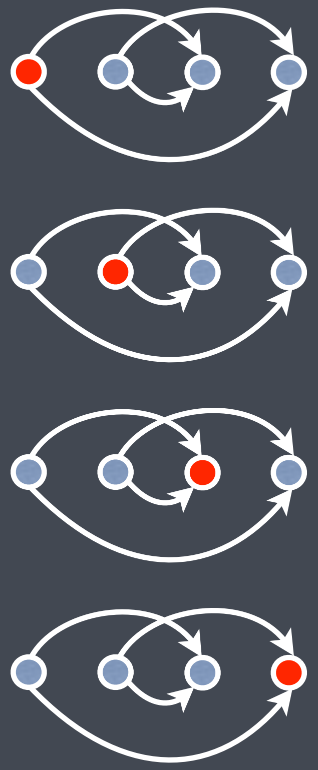
current values

guessed values

previous values



Registers:



1 -2	1 -2	1 -2
2 -1	2 -1	2 -1
1 -1	1 -1	1 -1
2 -2	2 -2	2 -2

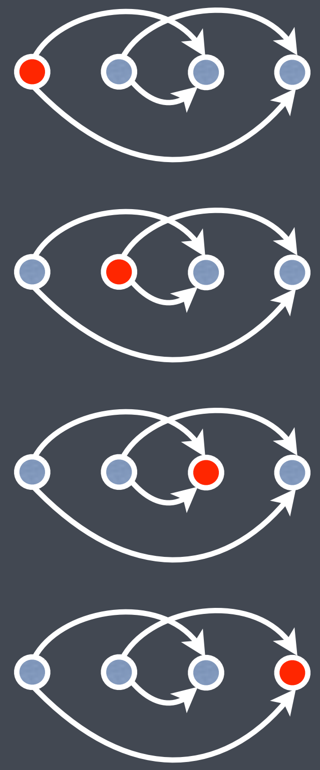
Sphere Automaton

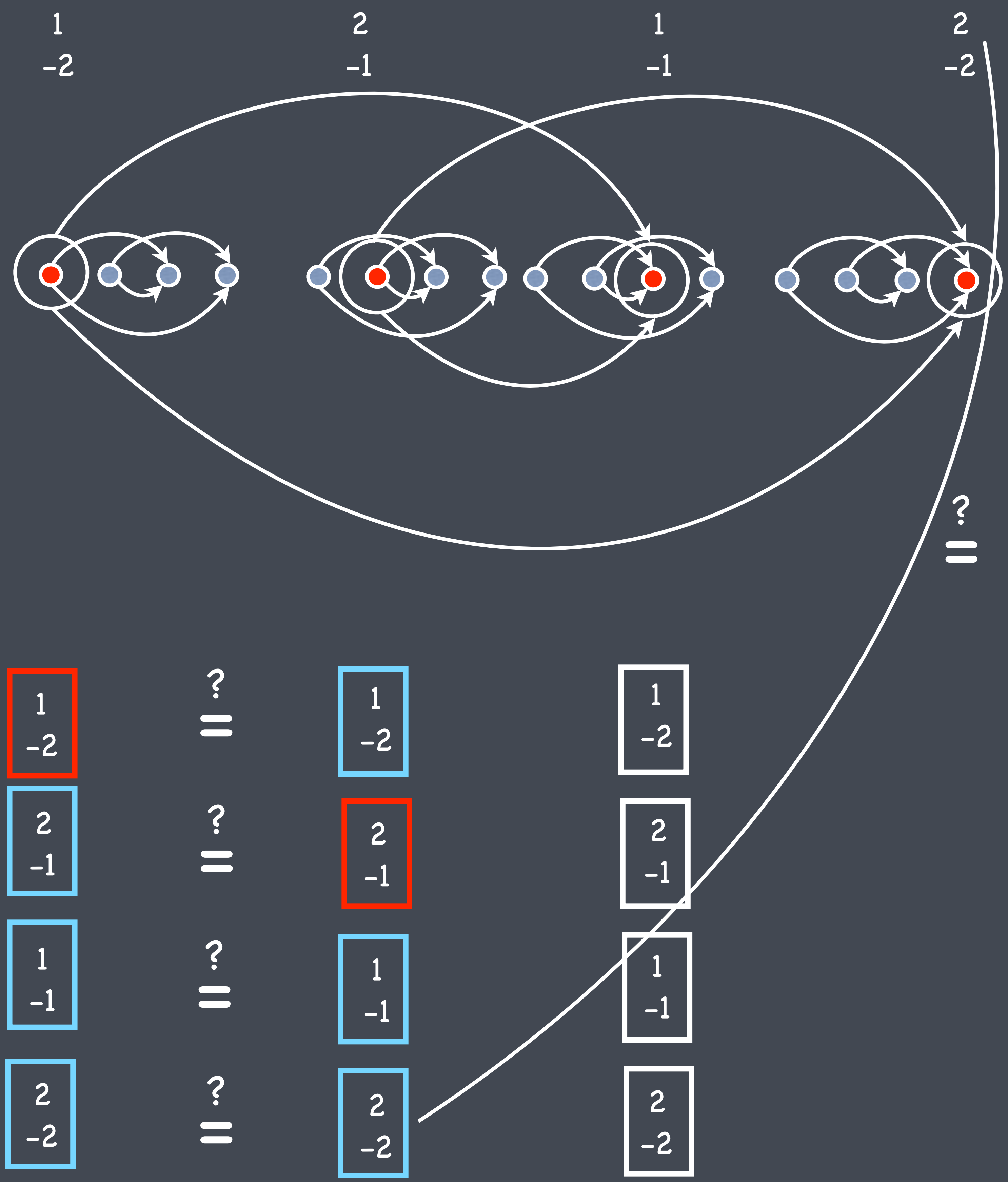
current values

guessed values

previous values

Registers:





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current values

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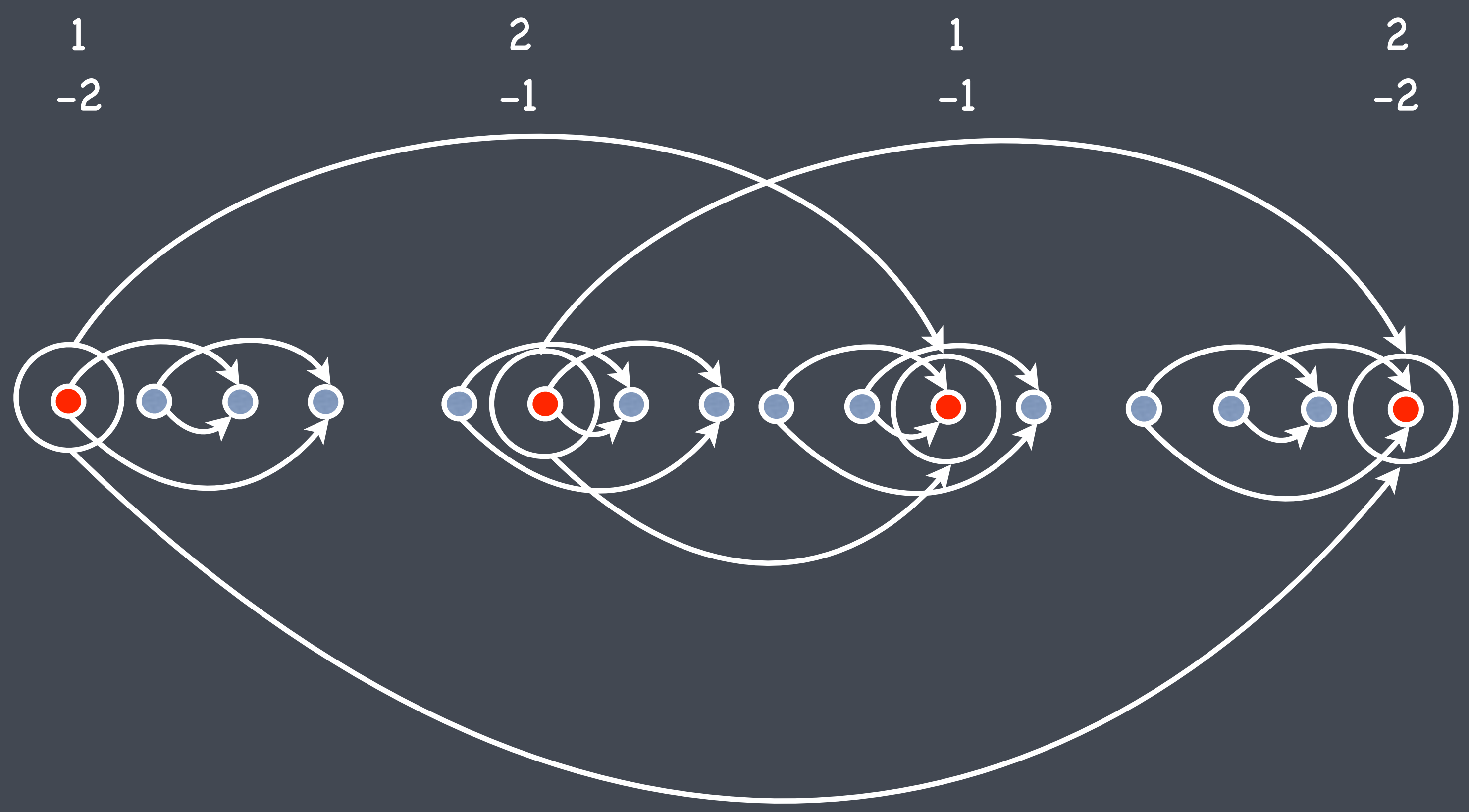
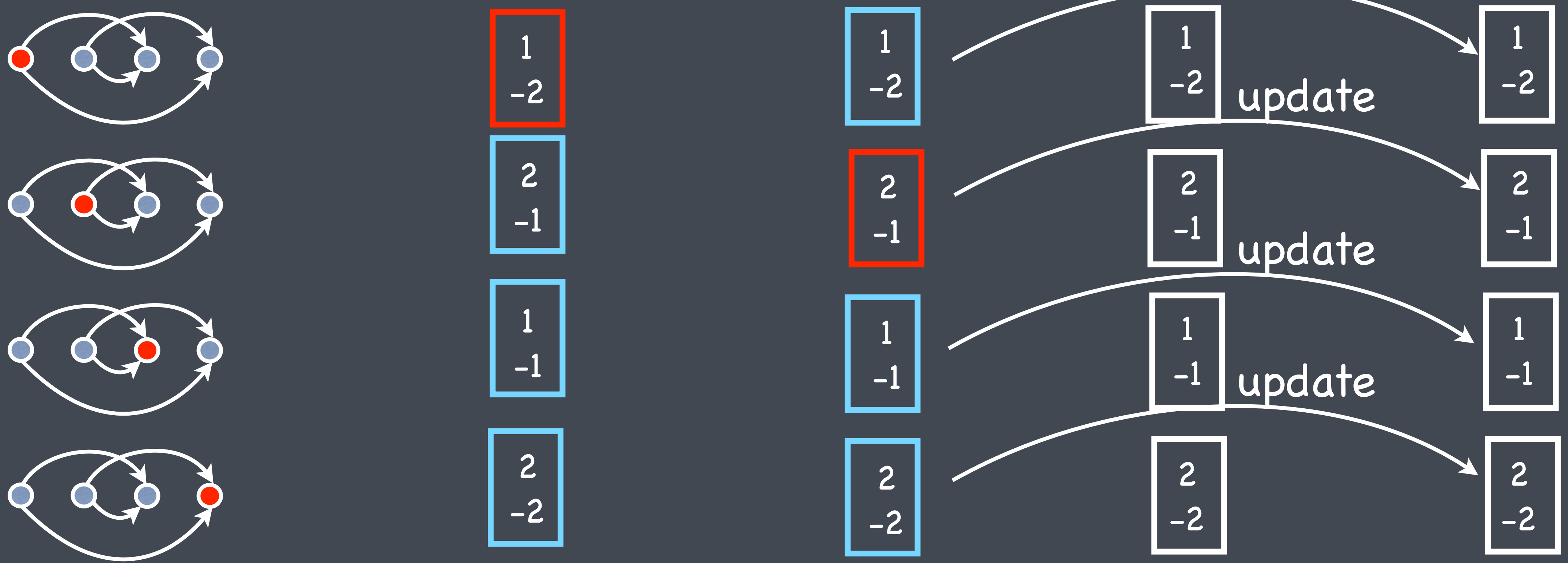
previous values



Registers:



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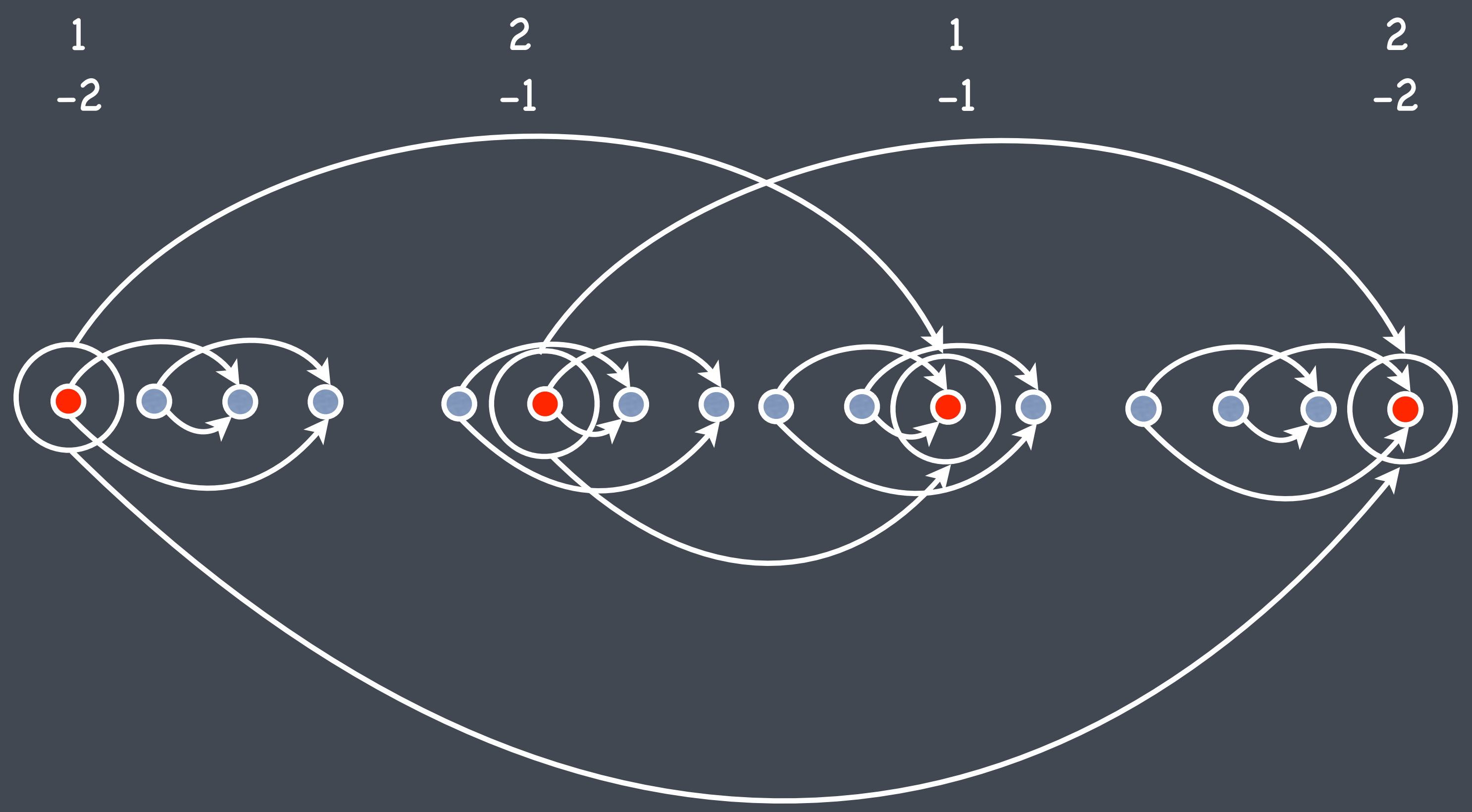

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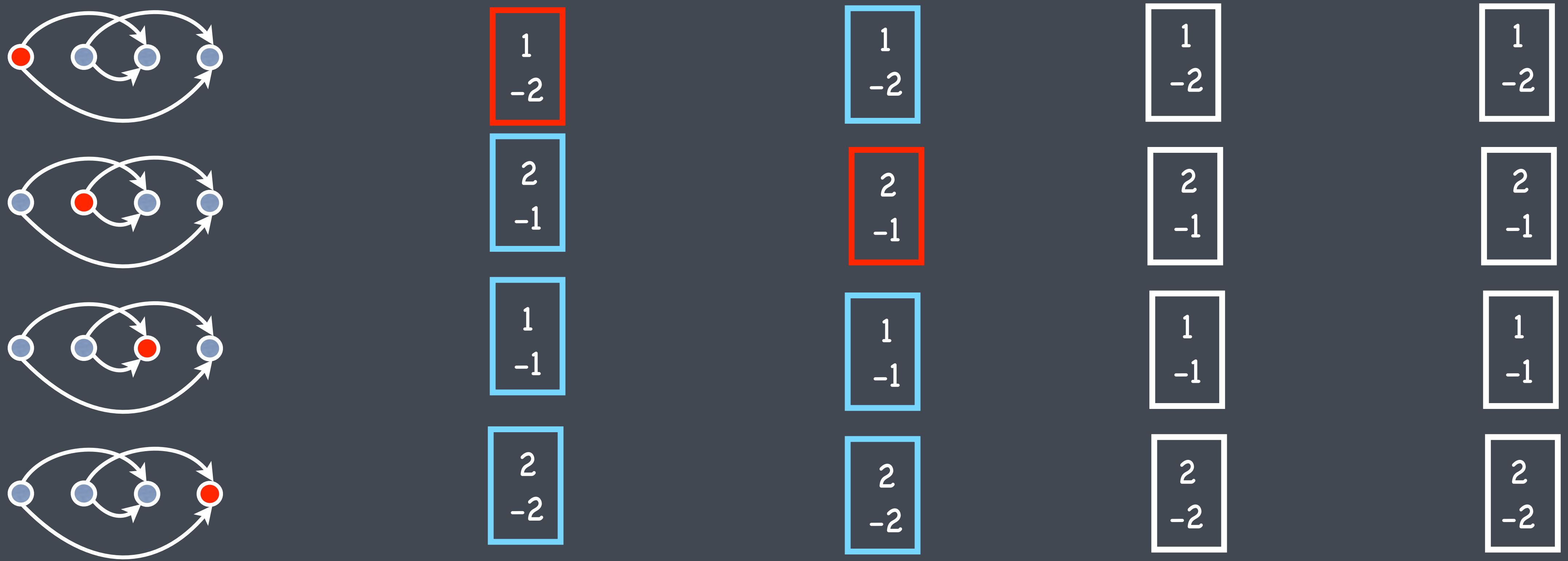
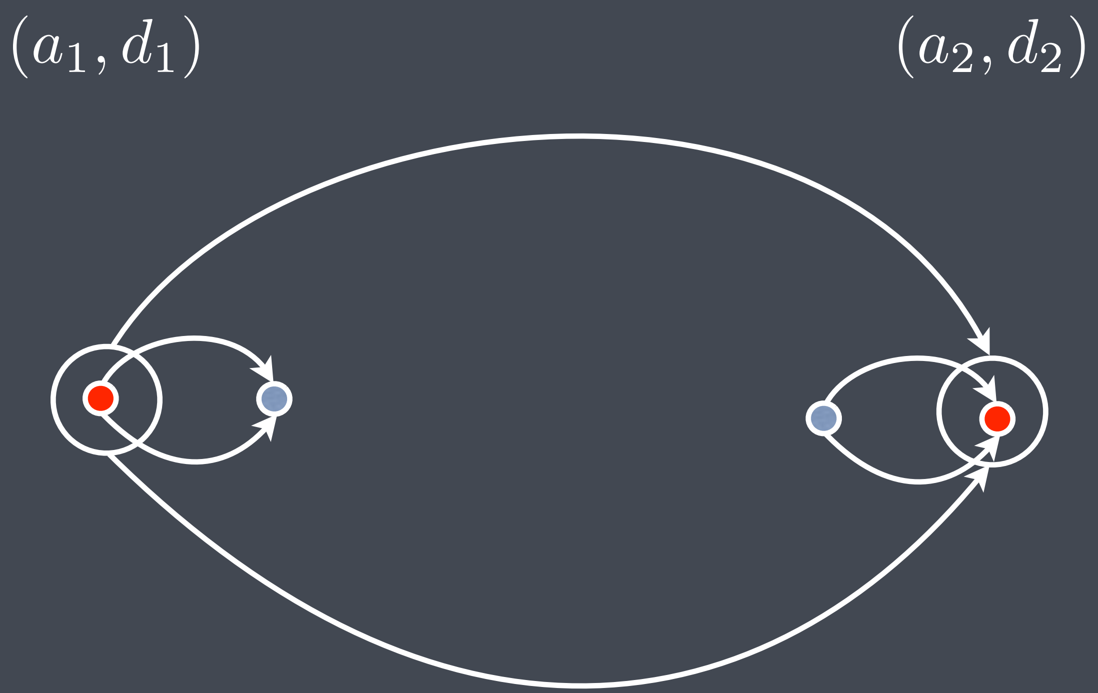


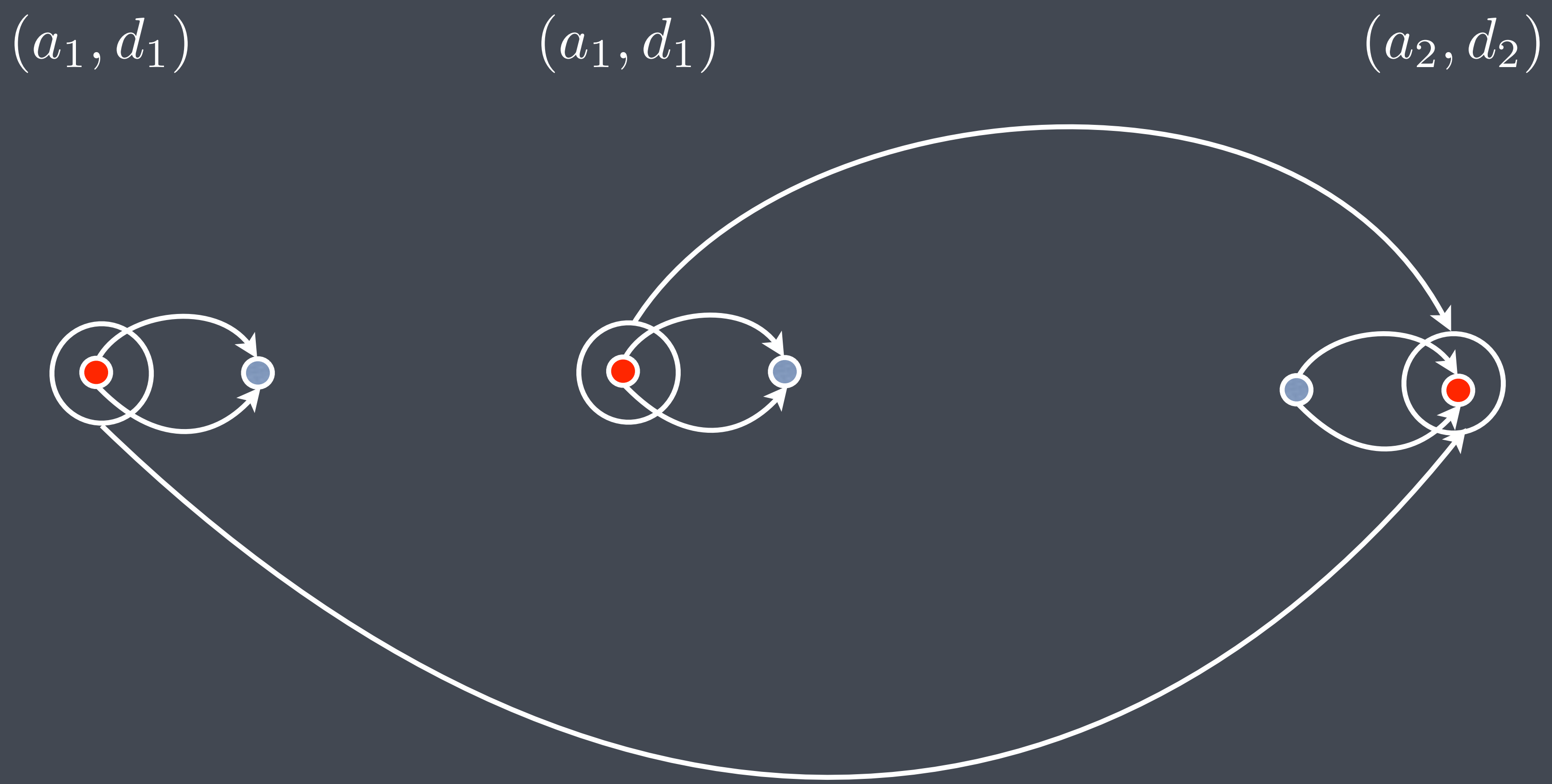
1 -2	1 -2	1 -2	1 -2
2 -1	2 -1	2 -1	2 -1
1 -1	1 -1	1 -1	1 -1
2 -2	2 -2	2 -2	2 -2

Sphere Automaton



How can we be sure that a cycle is closed?

Sphere Automaton



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Suppose it is not closed.

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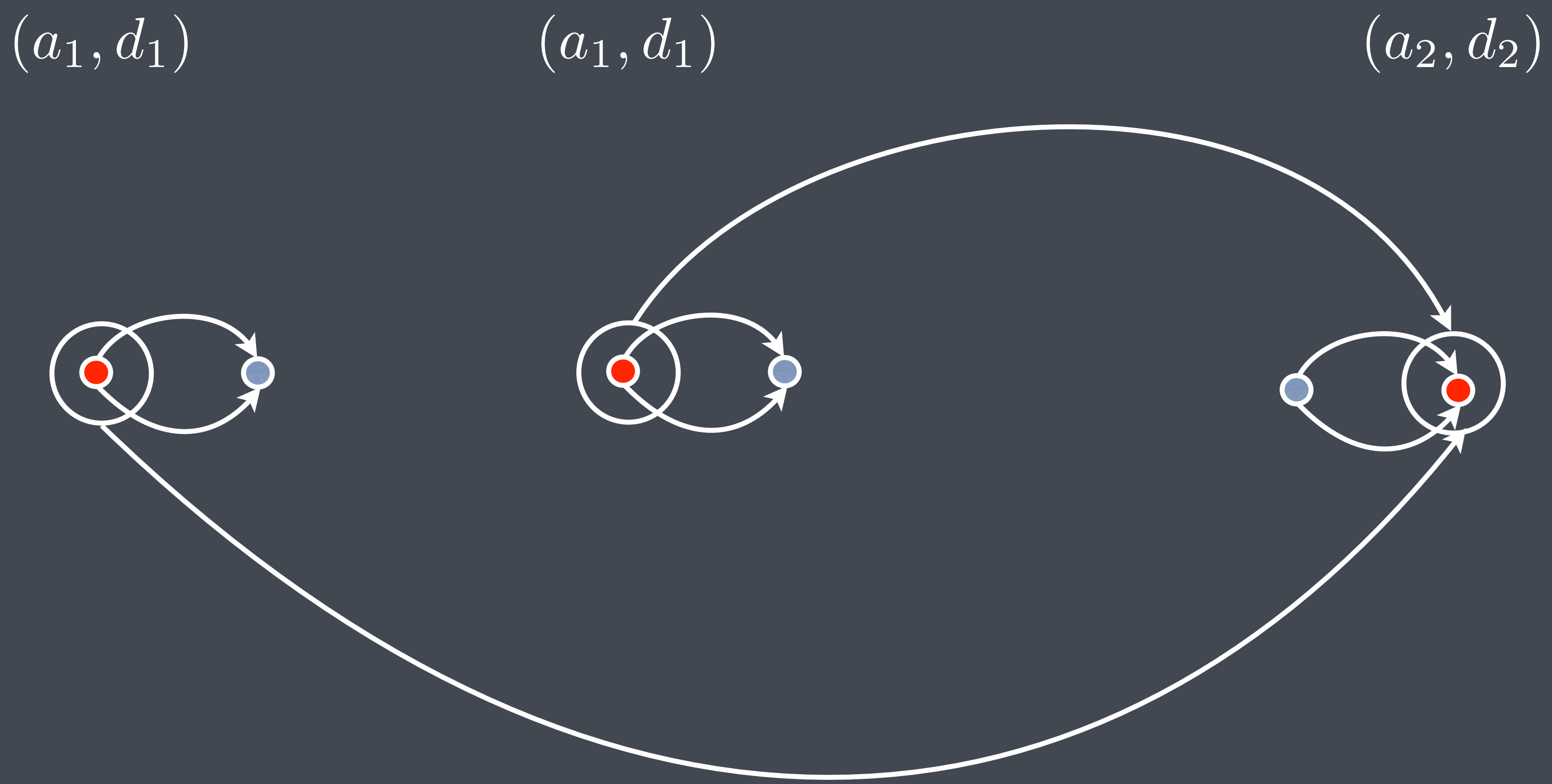

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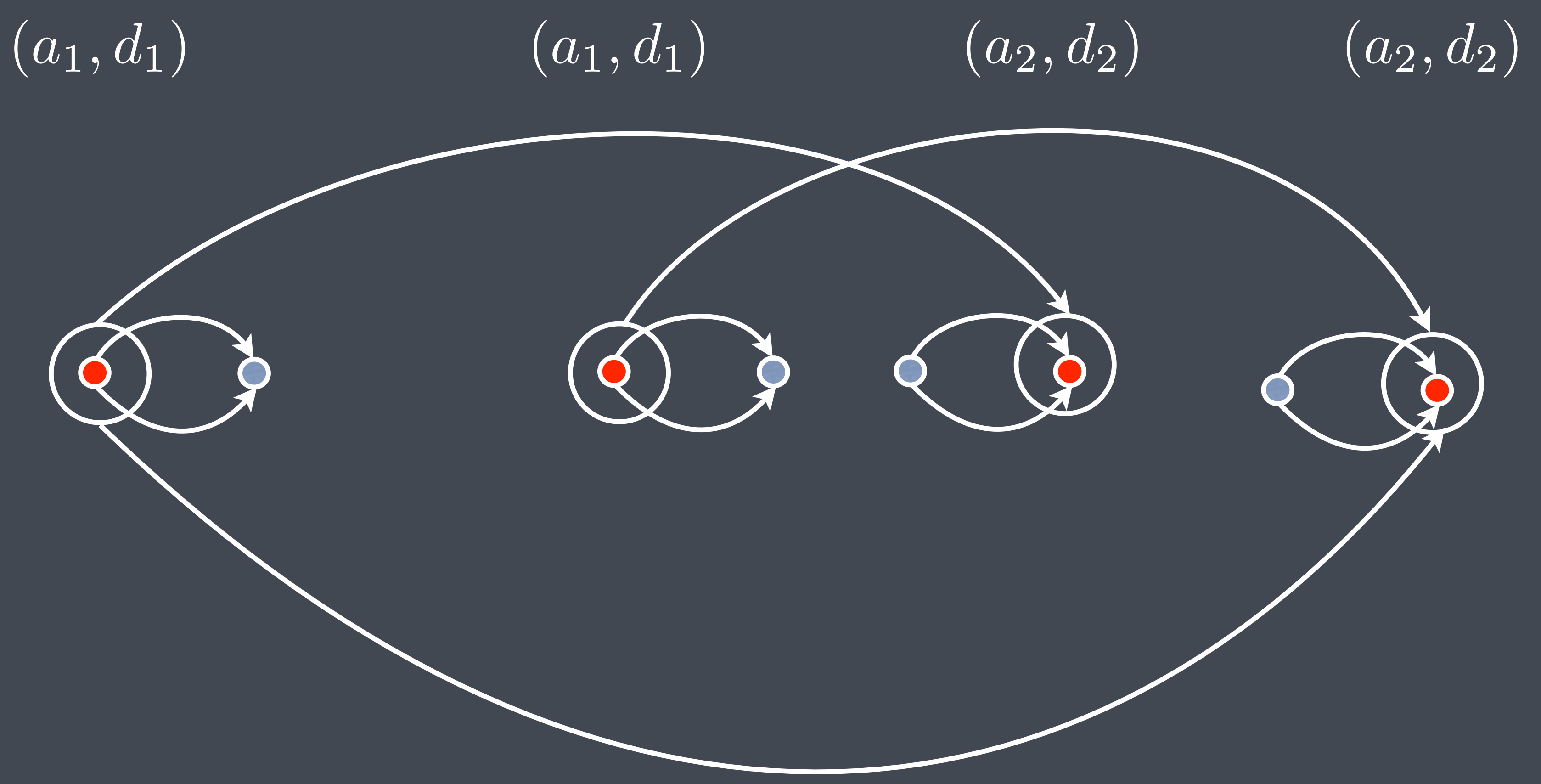

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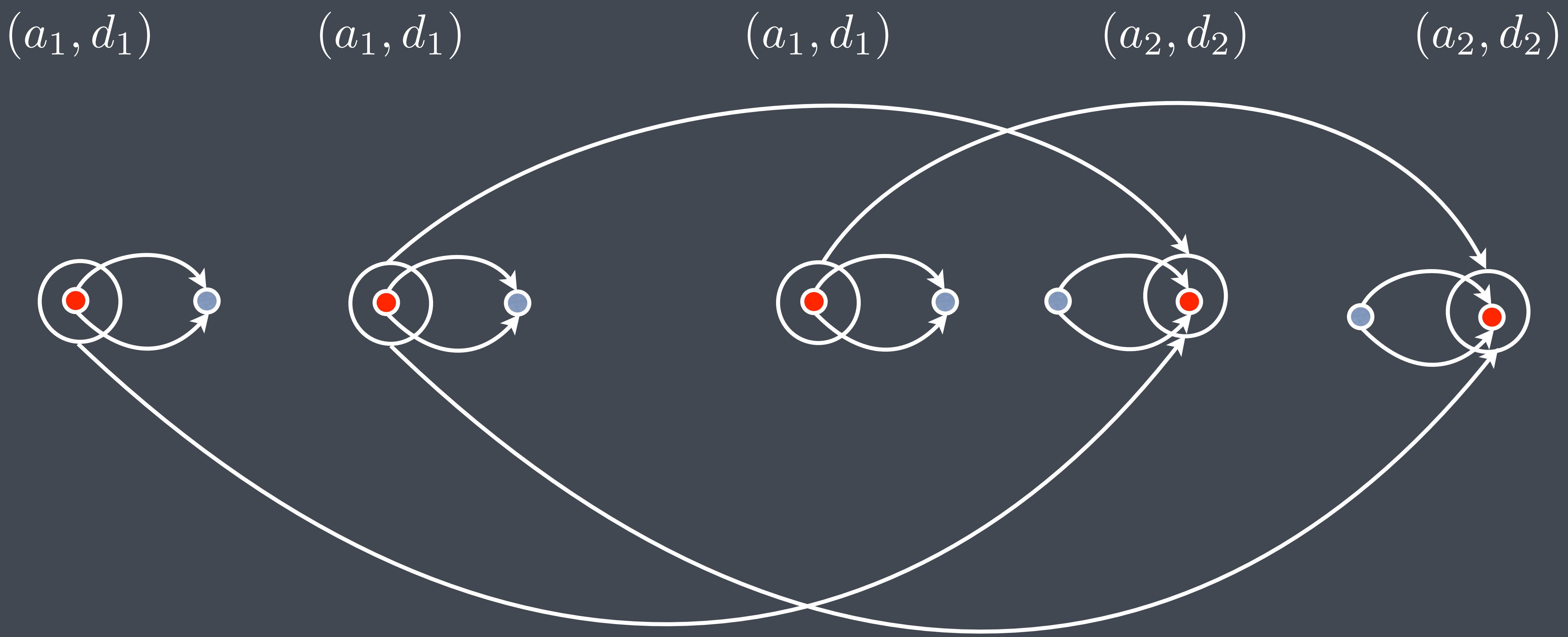

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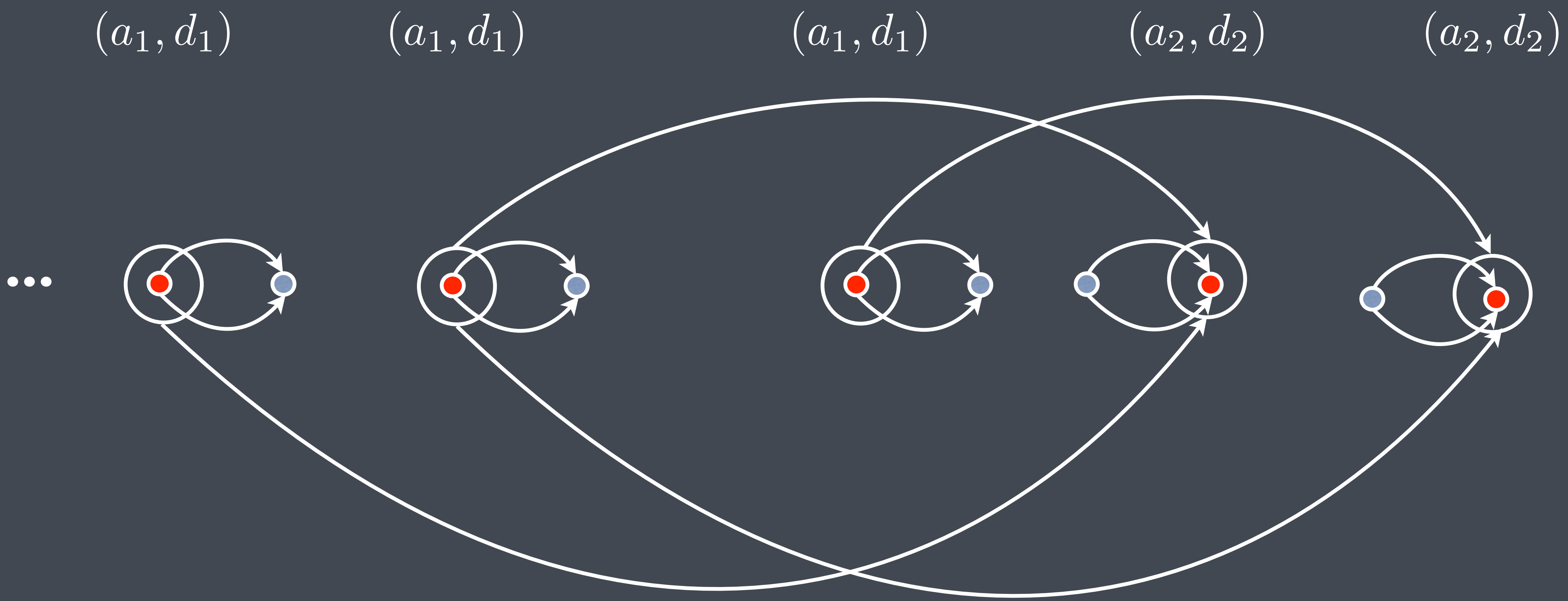

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=> infinite descending chain ↯

From Automata to Logic

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- Next: synthesize more practical automata
  => restricted specification languages
  => temporal logics