On the Verification Problem for Weak Memory Models

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[POPL'10]

Concurrent Programs

- Parallel processes with shared memory
- Interleaving (Sequentially Consistent) semantics:
  - Computations of different processes are shuffled
  - Program order is preserved for each process.

Relaxing the program order

$$\begin{array}{lcl} P_1 & : & \mathrm{write}(x,1) \quad ; \quad \mathrm{read}(y,0) \\ P_2 & : & \mathrm{read}(x,0) \end{array}$$

A scheduling for SC semantics: 3 steps

$$\begin{array}{lcl} P_1 & : & \mathrm{write}(x,1)_{(2)} \quad ; \quad \mathrm{read}(y,0)_{(3)} \\ P_2 & : & \mathrm{read}(x,0)_{(1)} \end{array}$$

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Allowing reordering of actions on different variables: 2 steps !

$$\begin{array}{lcl} P_1 & : & \mathrm{read}(y,0)_{(1)} \quad ; \quad \mathrm{write}(x,1)_{(2)} \\ P_2 & : & \mathrm{read}(x,0)_{(1)} \end{array}$$

$\Rightarrow$ *Weak Memory Models*

Program Order Relaxations: Classification

- $W \rightarrow R$: Write to Read

  write (x) ; read (y) $\mapsto$ read (y) ; write (x)

  $\Rightarrow$ TSO model (Total Store Ordering)

- (+) $W \rightarrow W$: Write to Write

  $\Rightarrow$ PSO model (Partial Store Ordering)

- (+) $R \rightarrow R/W$: Read to Read/Write

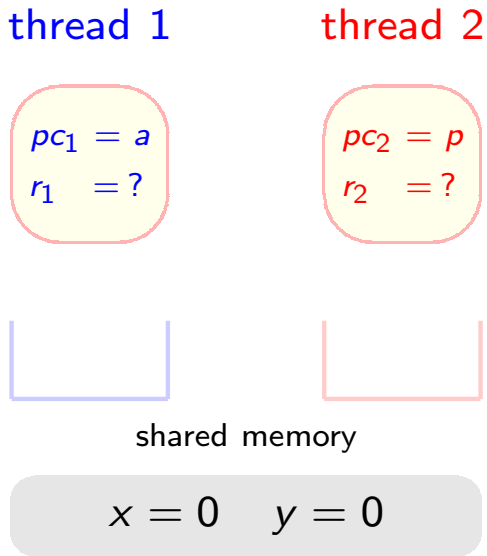
  $\Rightarrow$ $\sim$RMO model (Relaxed Memory Ordering)

Relaxation ⇒ Potential Bad Behaviors

$x = y = 0$

thread 1	thread 2
a: $y = 1$	p: $x = 1$
b: $r_1 = x$	q: $r_2 = y$
c: if($r_1 == 0$) {	s: if($r_2 == 0$) {
d: ...	t: ...
}	}

1- Initial state



Dekker's mutual exclusion protocol. Fails under Write to Read relaxation.

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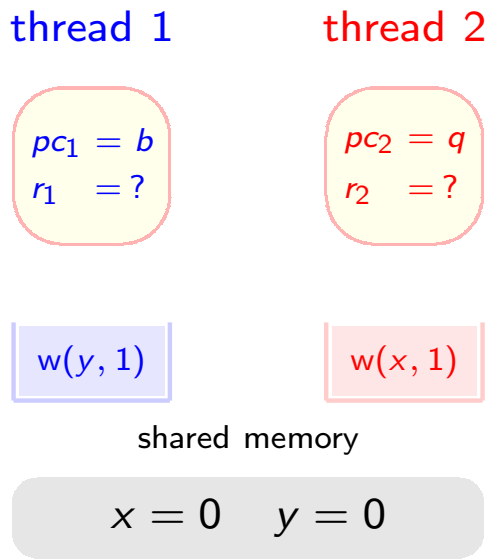
2- Writes are postponed



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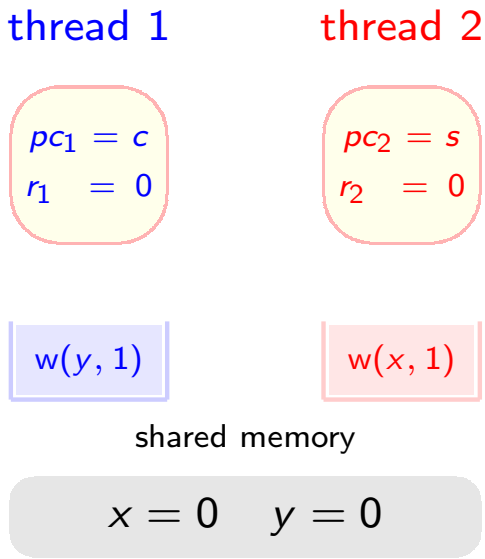
3- Reading from memory



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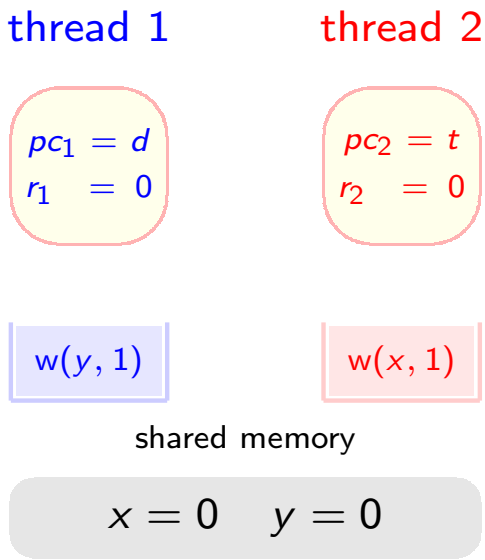
4- Accessing critical sections



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Verification Problems

For a memory model μ, a program P, and a (control + memory) state s

- State Reachability Problem (Safety)

  s is reachable in P ?

- Repeated State Reachability Problem (Liveness)

  s is reachable infinitely often in a computation of P ?

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- Nontrivial for weak memory models:

  $Paths_{\mu}(P) = Closure_{\mu}(Paths_{SC}(P))$ *is nonregular*

Results

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  $$W \rightarrow R \text{ (TSO) } \textit{and } W \rightarrow R/W \text{ (PSO)}$$

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- Decidability/Complexity:

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- Undecidability for W $\rightarrow$ R/W + R $\rightarrow$ R/W:

  Reduction of the Post Correspondence Problem.

An operational model for TSO

- Finite number of shared variables $\{x, y, x_1 ...\}$
- Finite data domain $\{d, d_1, d_2, ...\}$
- Finite number of finite-control processes $P_1, \ldots, P_n$ with operations:

$$Nop, Write(x, d), Read(x, d), AtomicRW(x, d_1, d_2)$$

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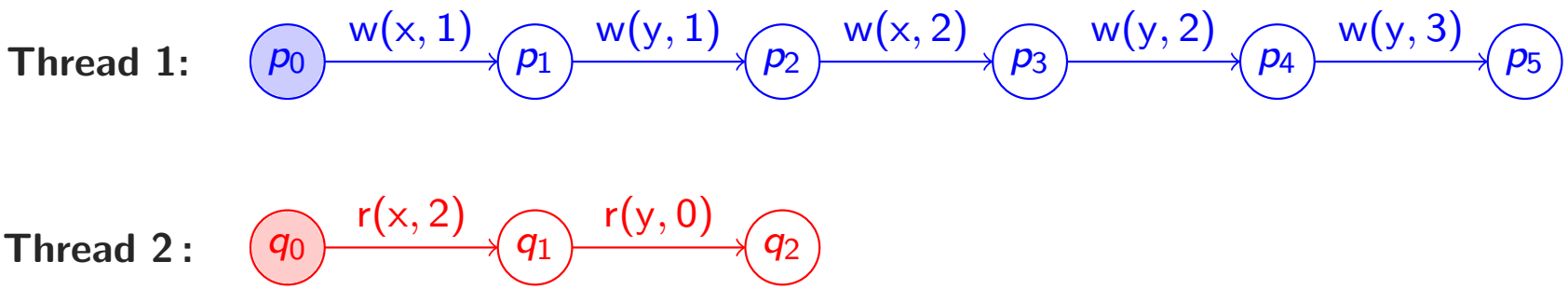
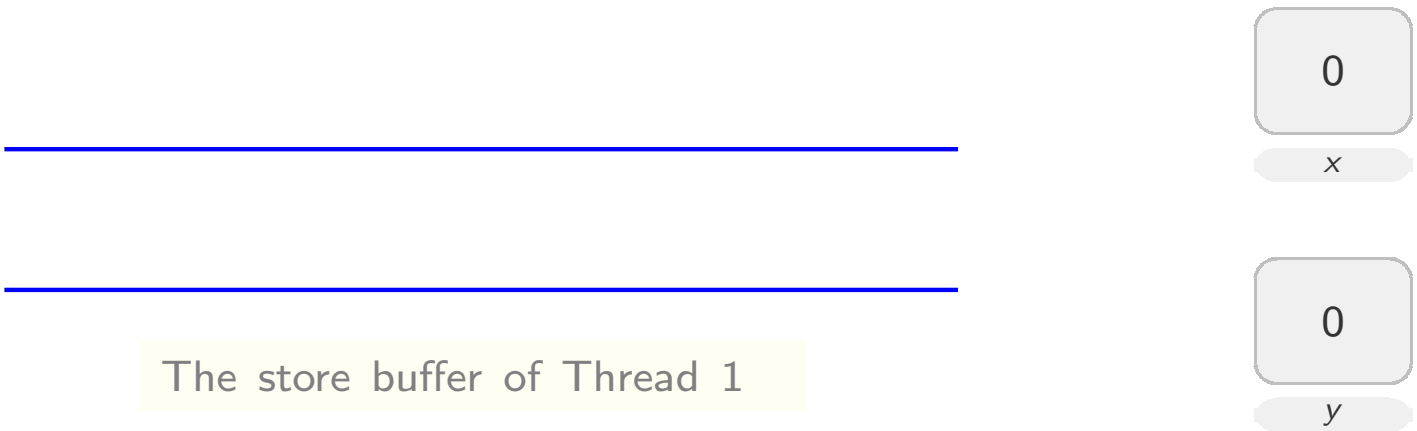
- Each process has a FIFO buffer
- Configuration = control states + memory state + buffers contents
- Write(x,d) is sent to the buffer
- Memory update = execution of a Write taken from some buffer
- Read(x,d) is executed either if
  - The last Write to x in the buffer is Write(x,d) (Read Own Write)
  - The buffer does not contain a Write to x, and $Memory(x) = d$
- $AtomicRW(x, d_1, d_2)$ requires that the buffer is empty ($\sim$ fence)

From W $\longrightarrow$ R systems to Lossy Channel Systems



Model: The store buffers are considered as perfect FIFO channels



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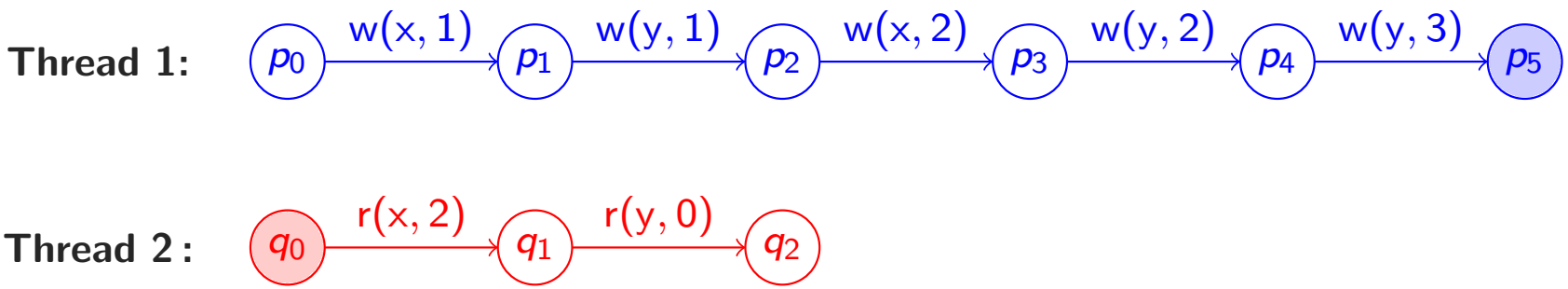

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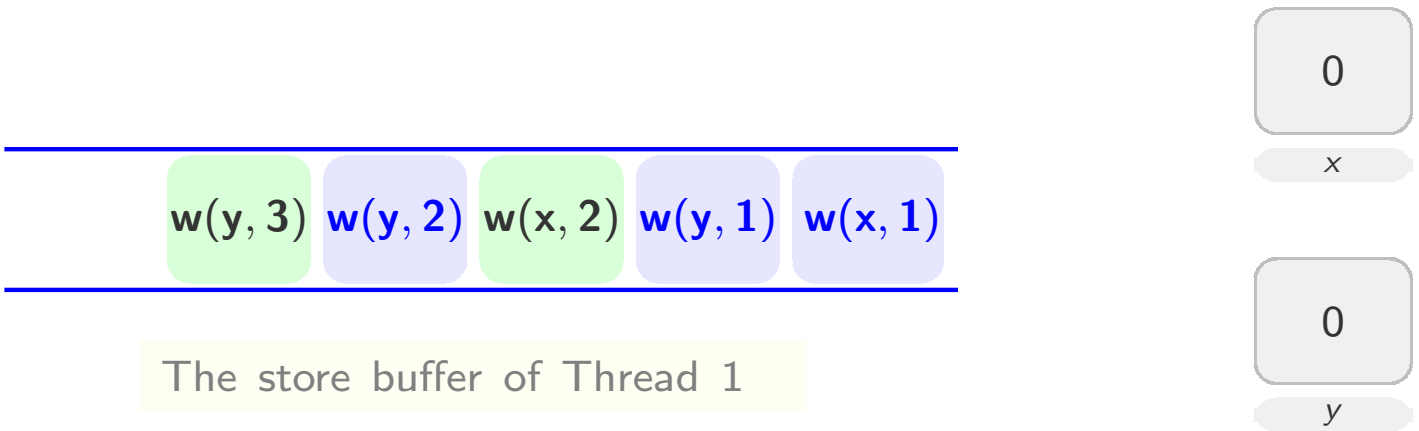

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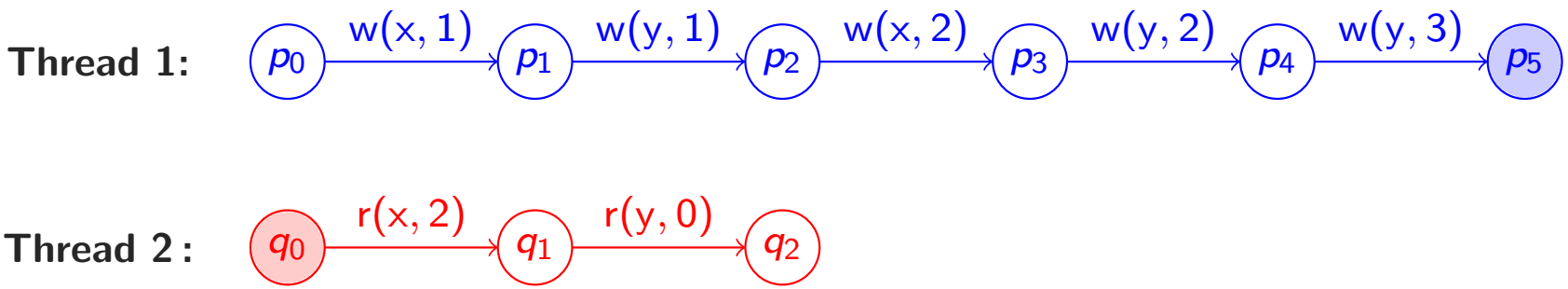

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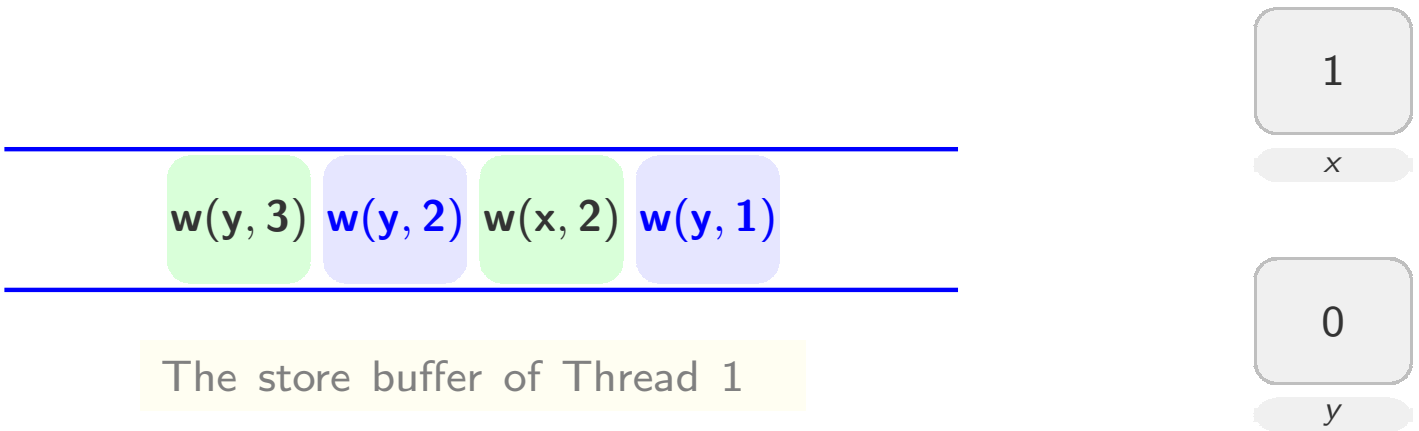

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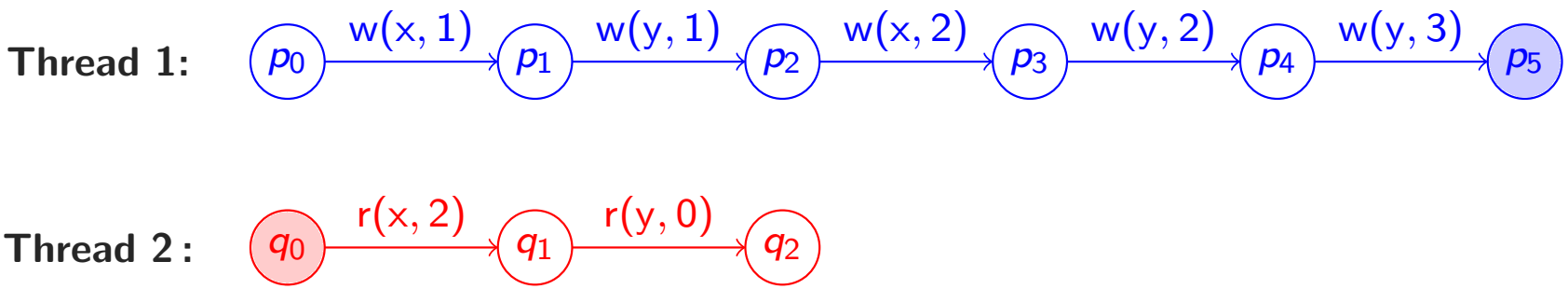

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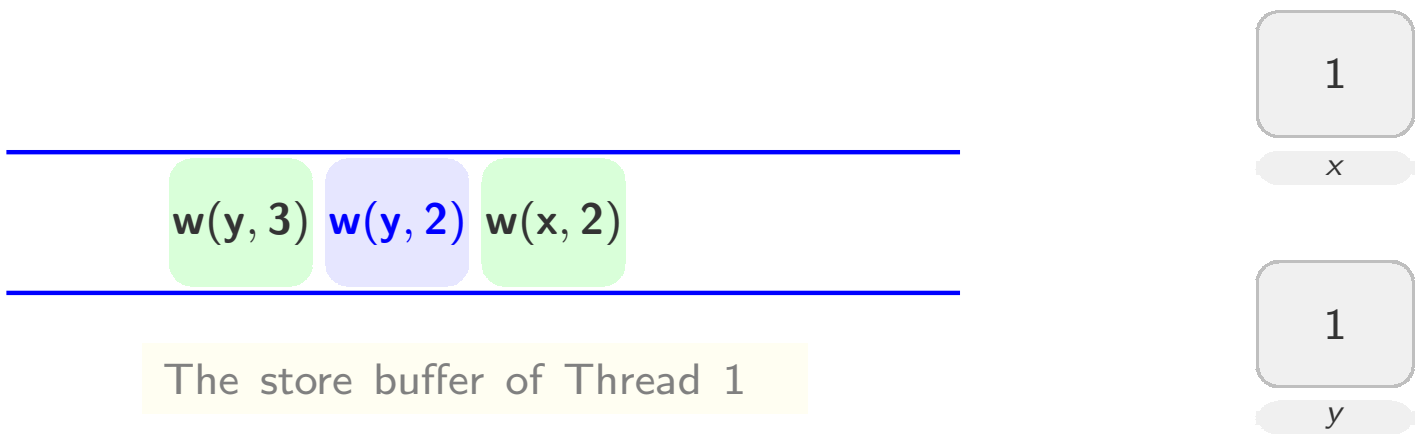

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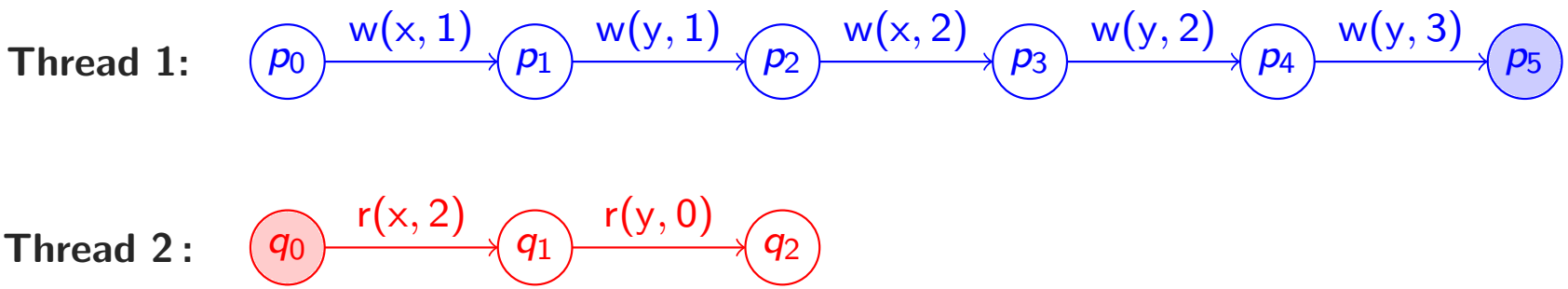

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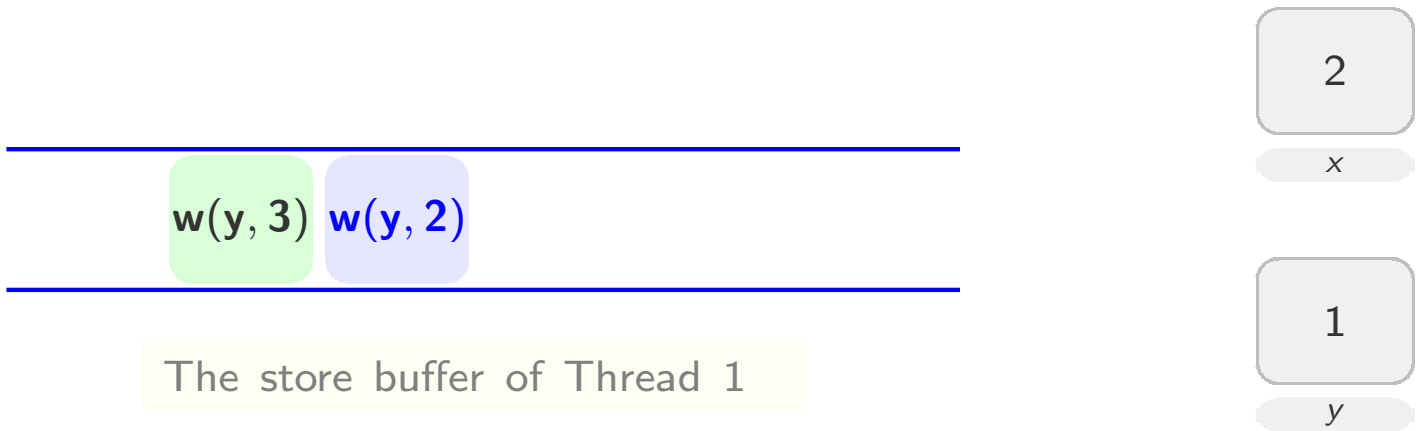

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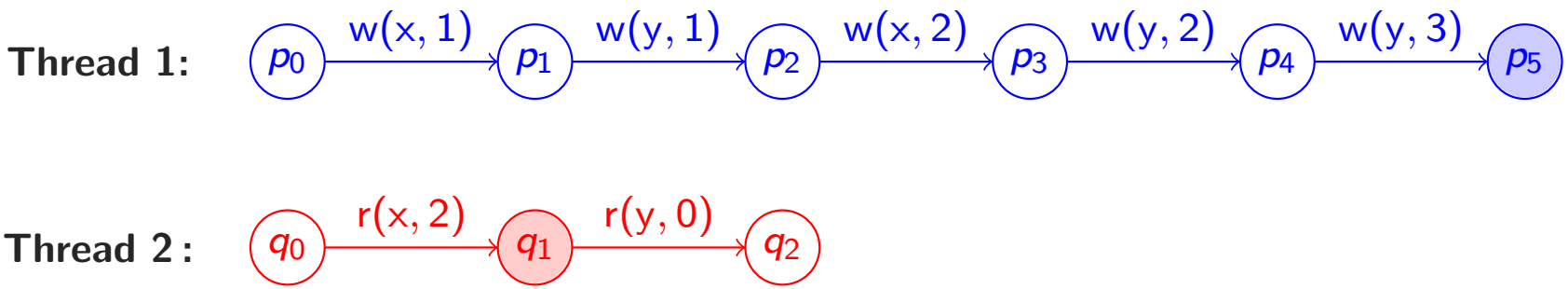

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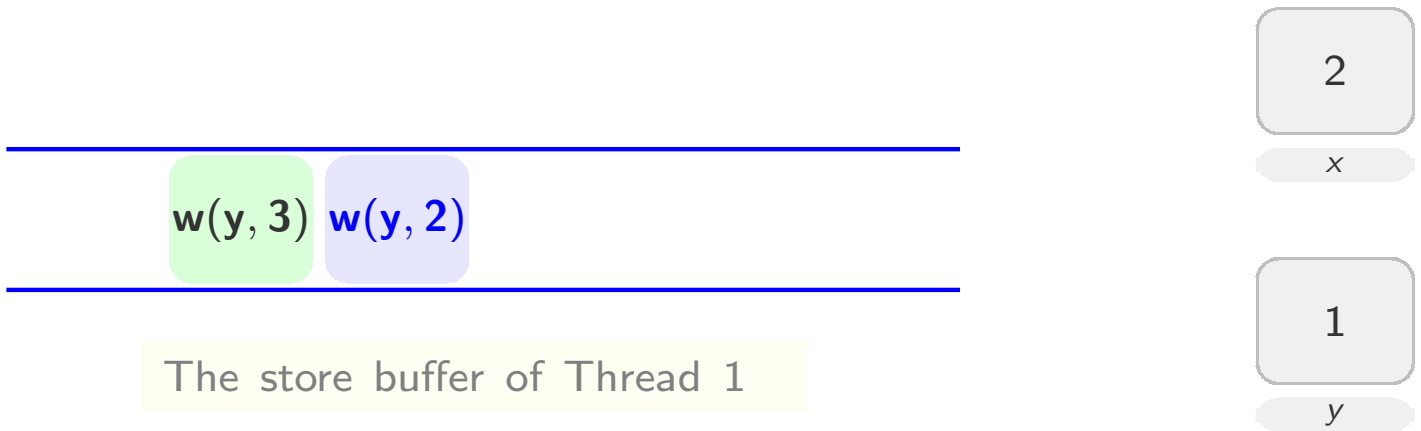

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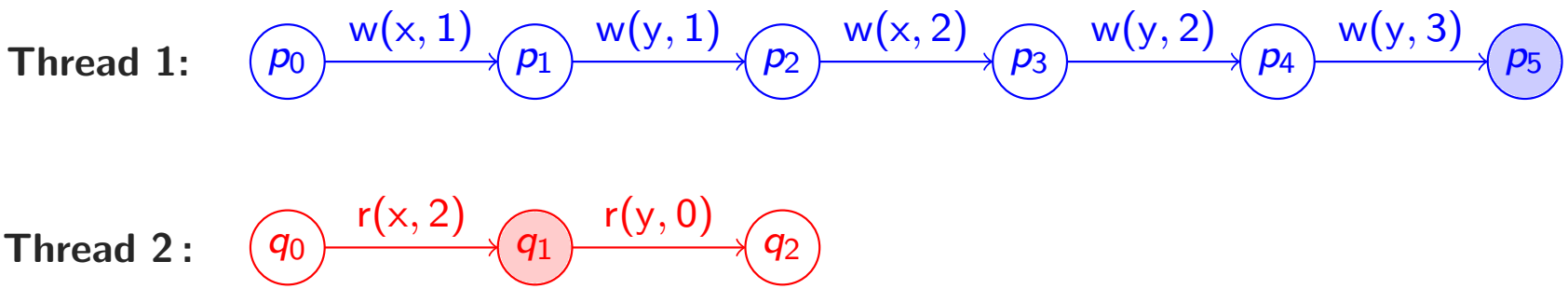

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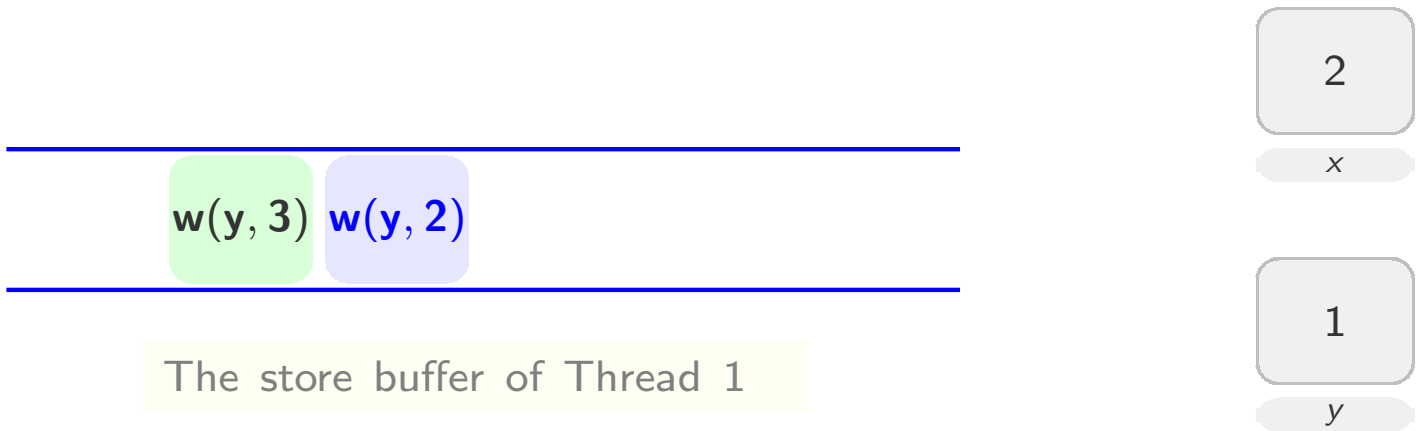

Deadlock

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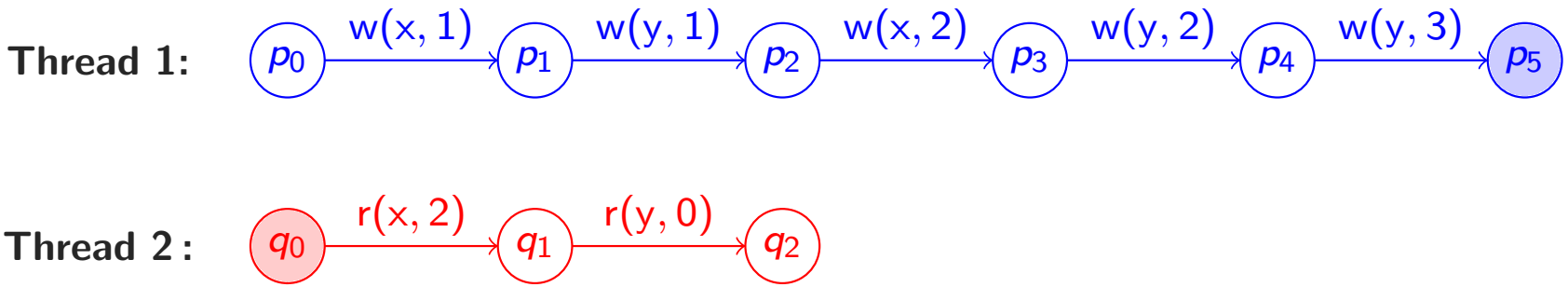

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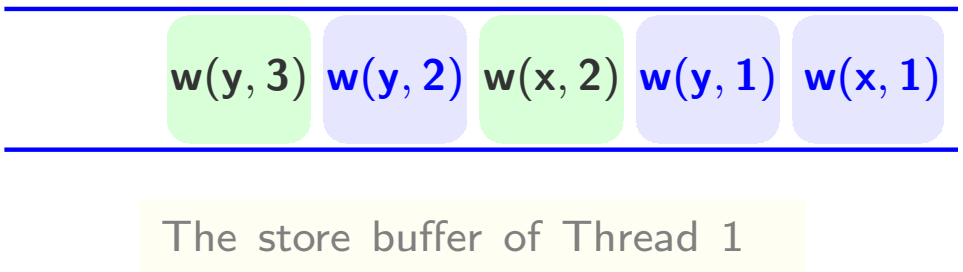

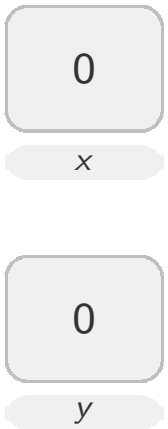

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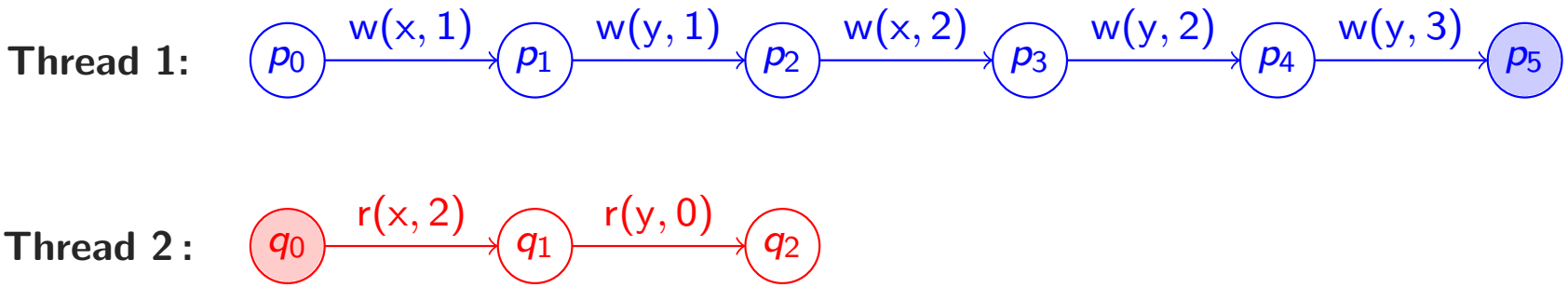

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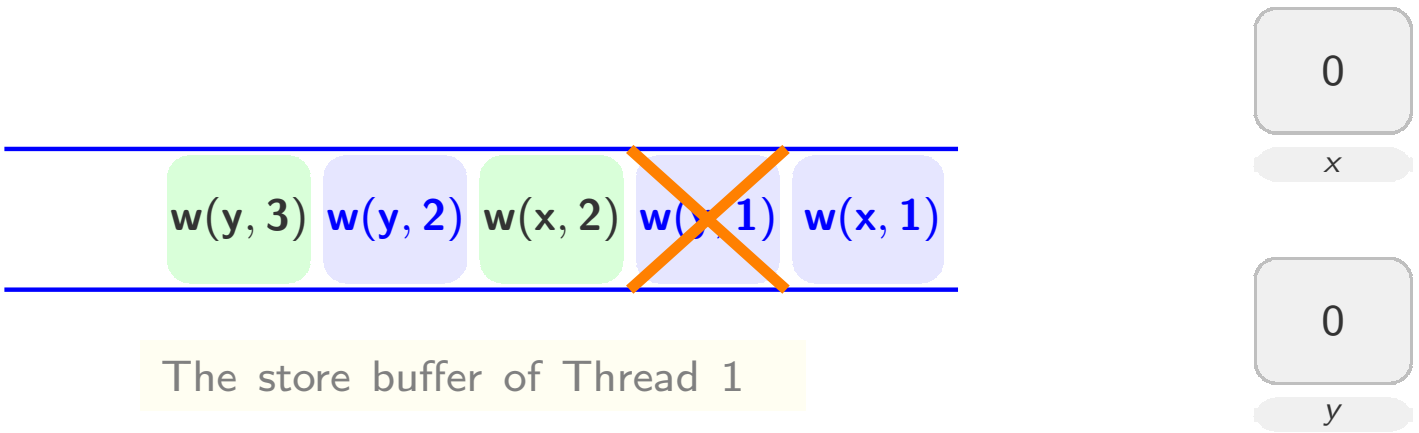

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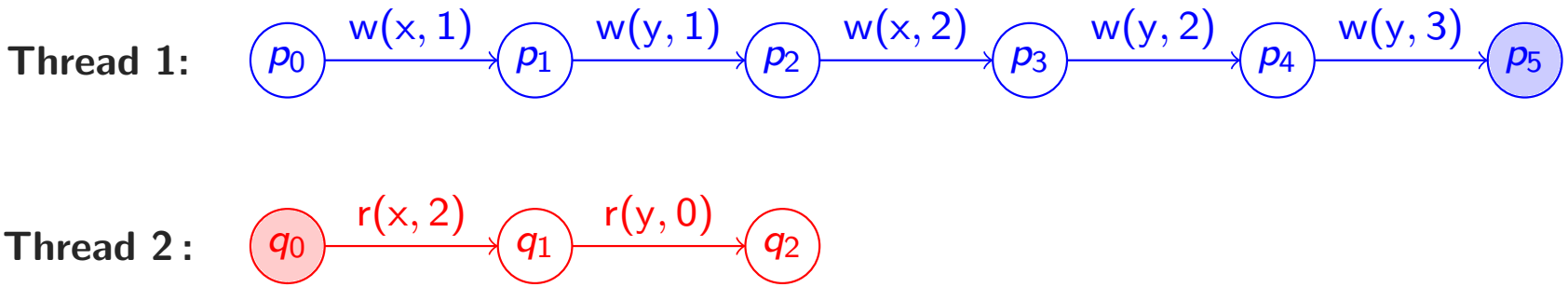

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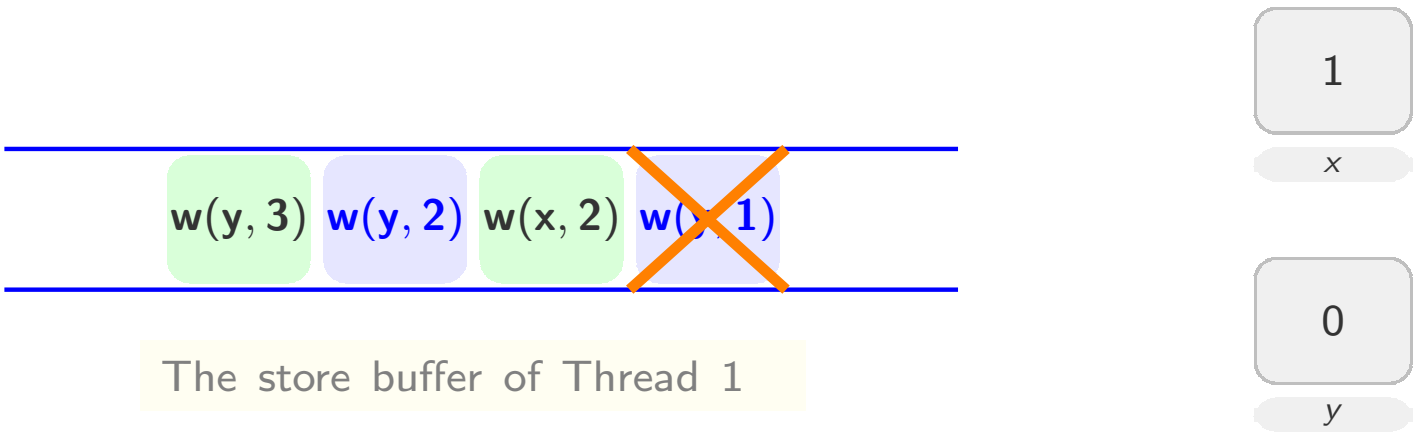

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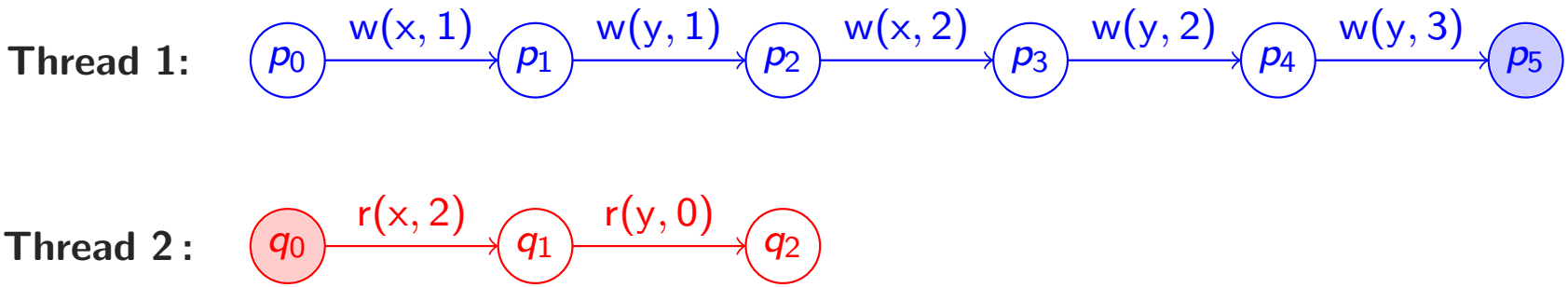

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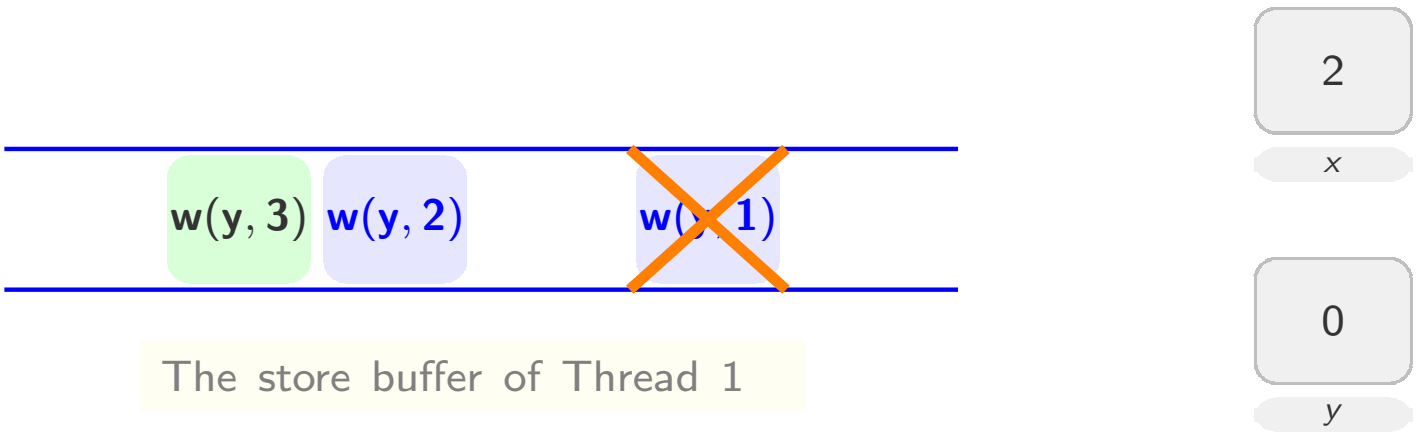

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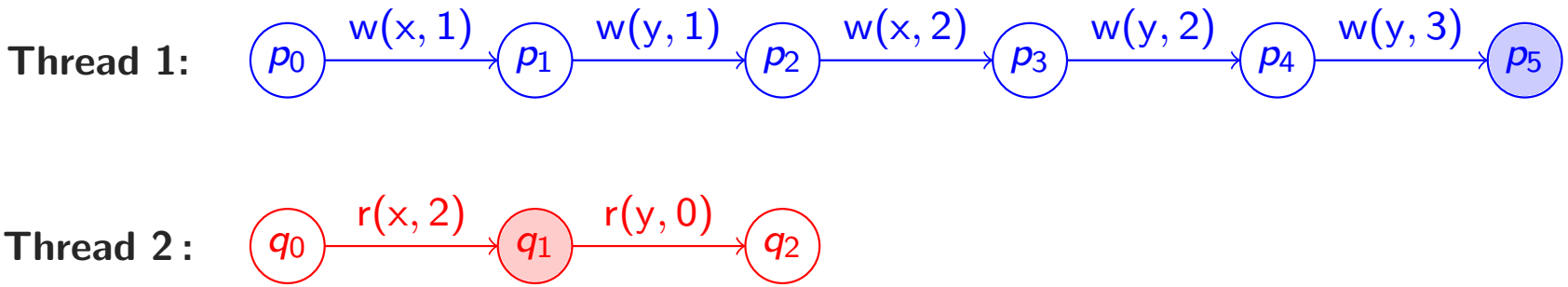

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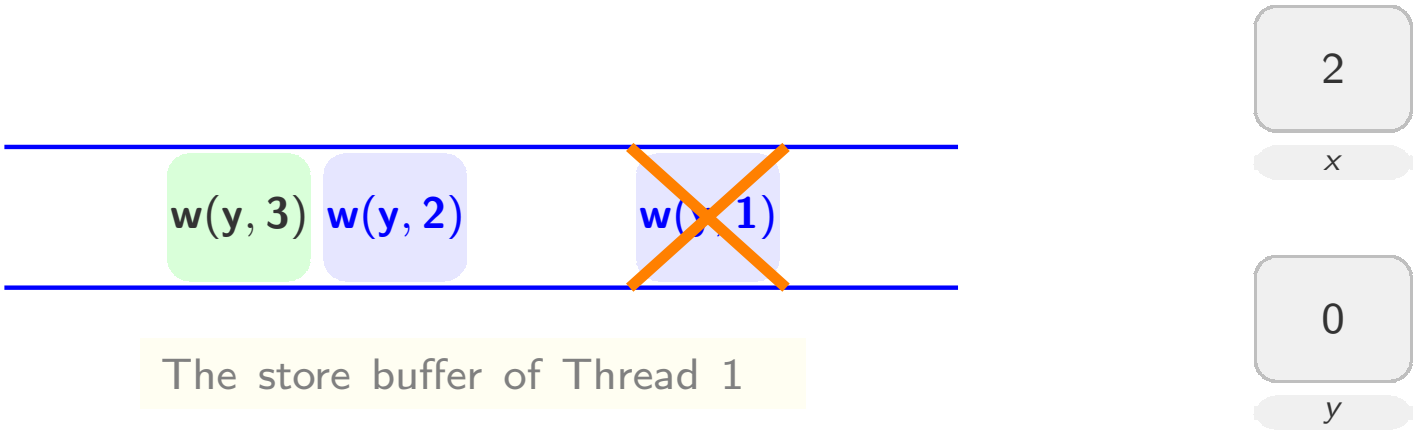

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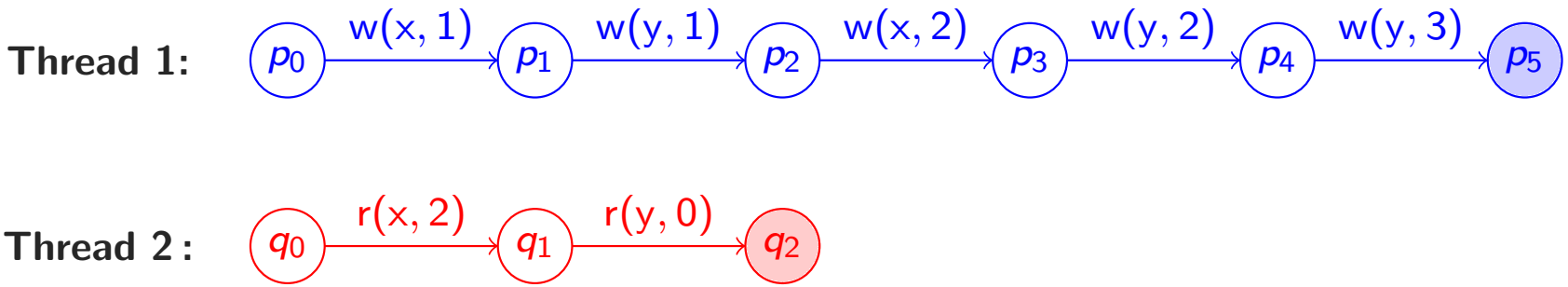

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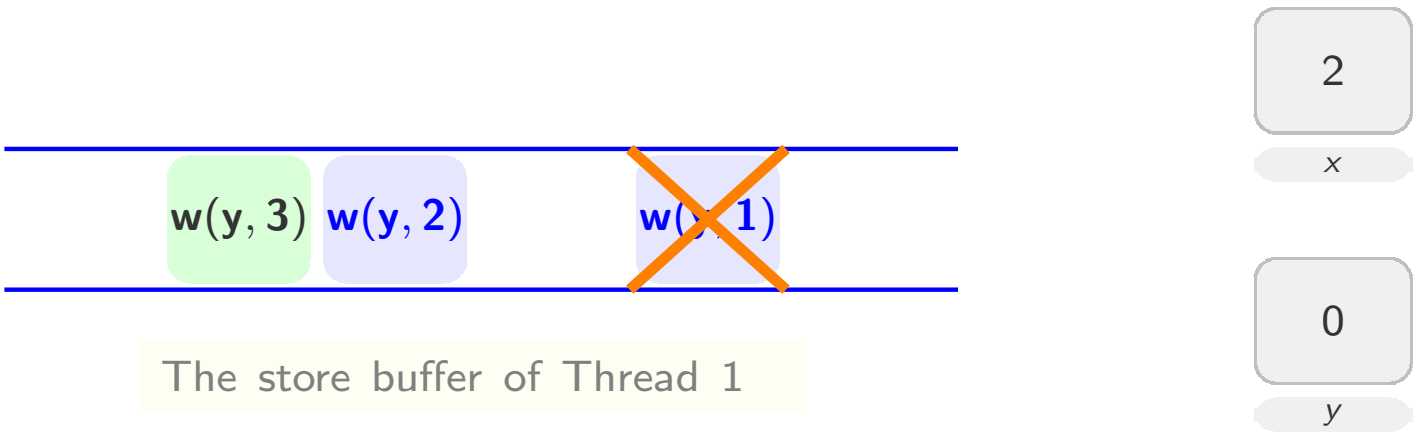

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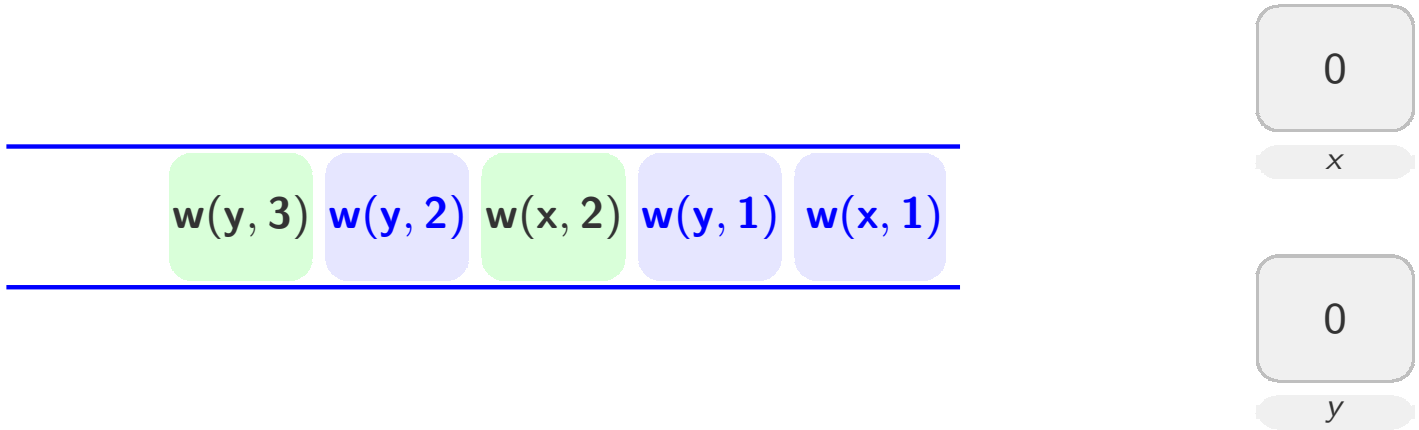
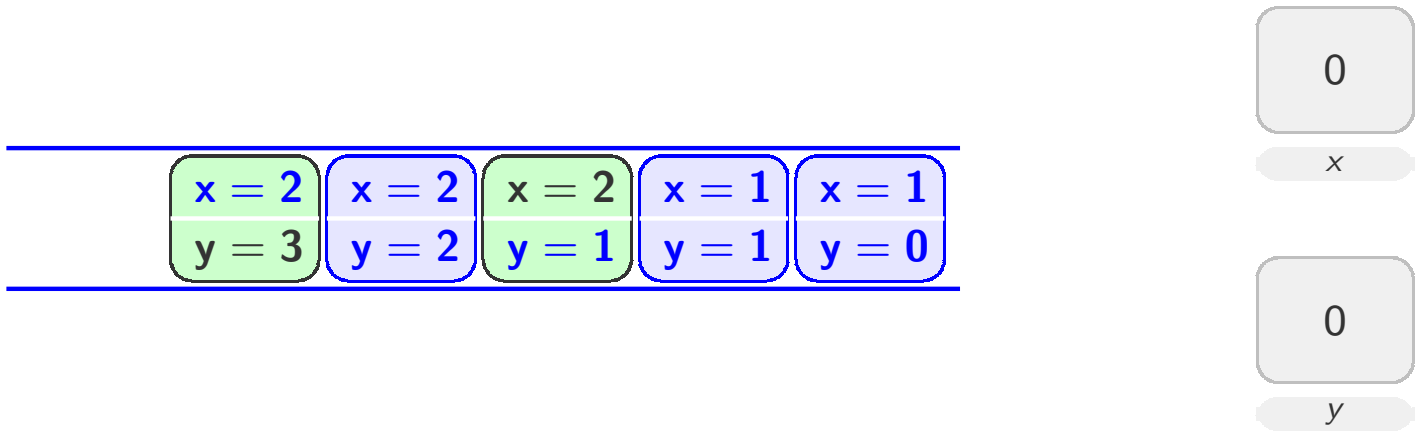


Channel= Sequence of memory states + Lossyness



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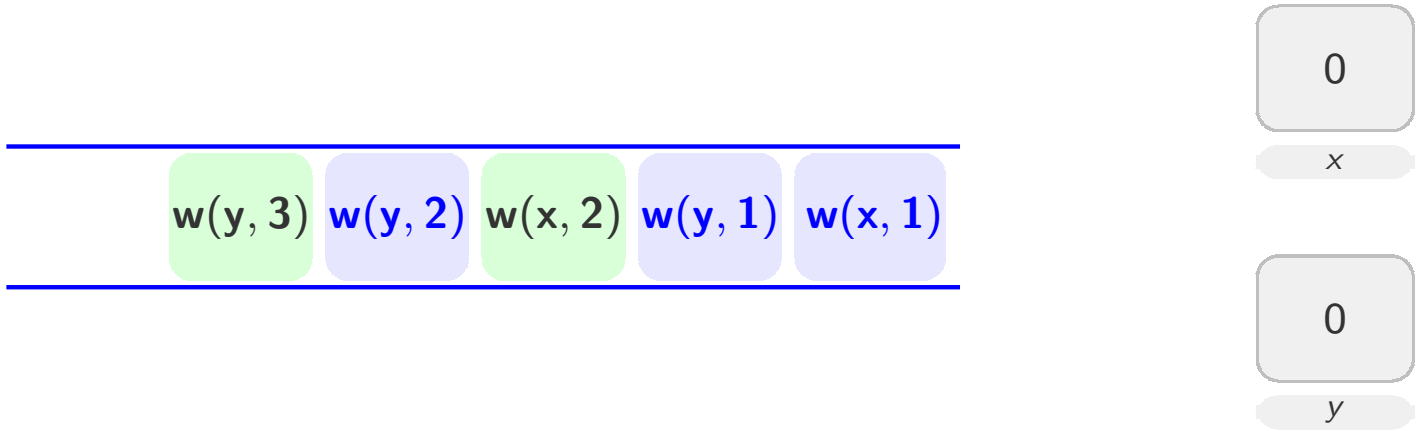

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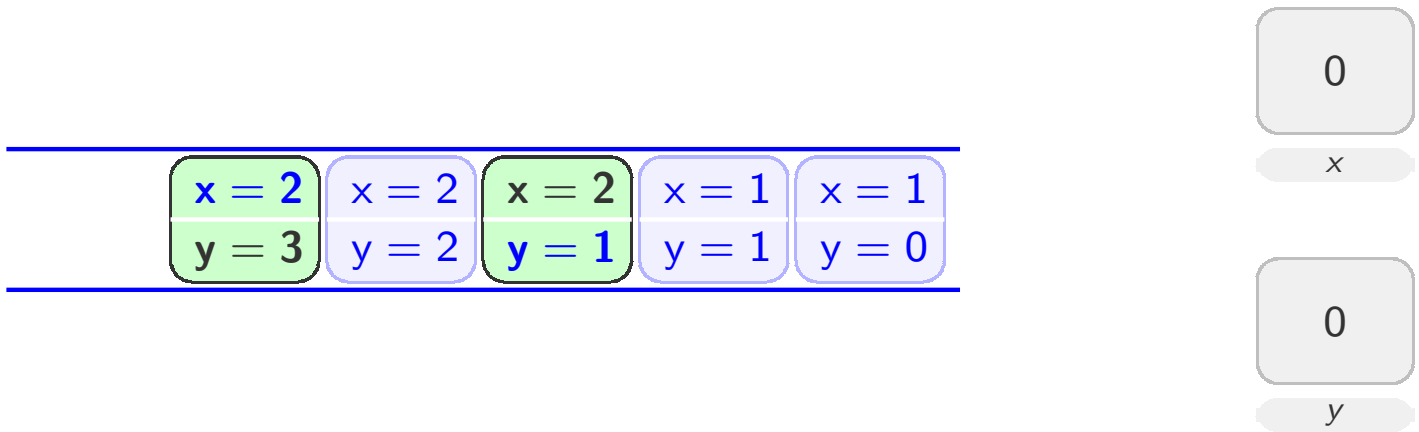

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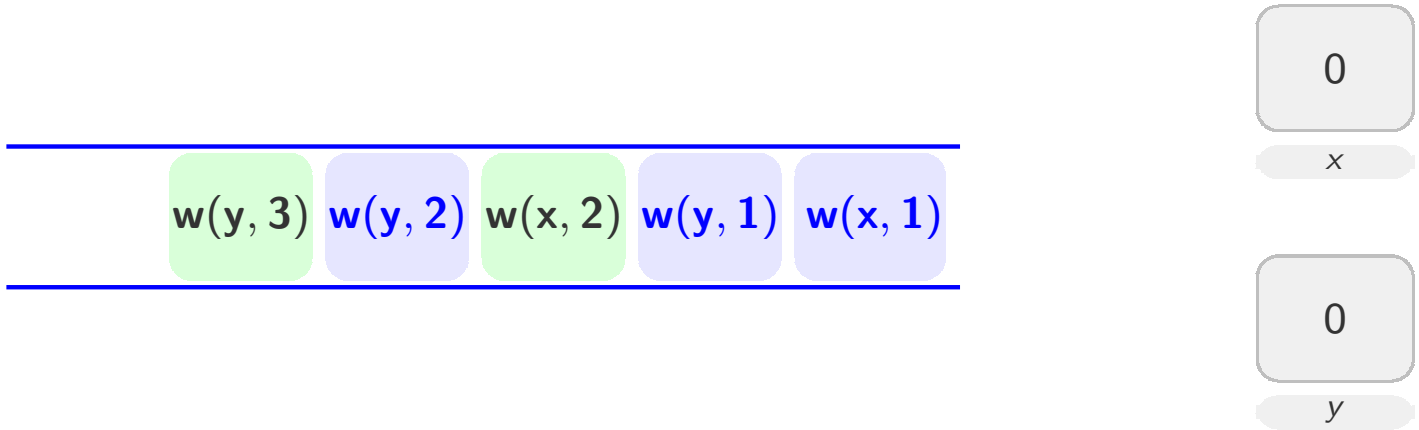

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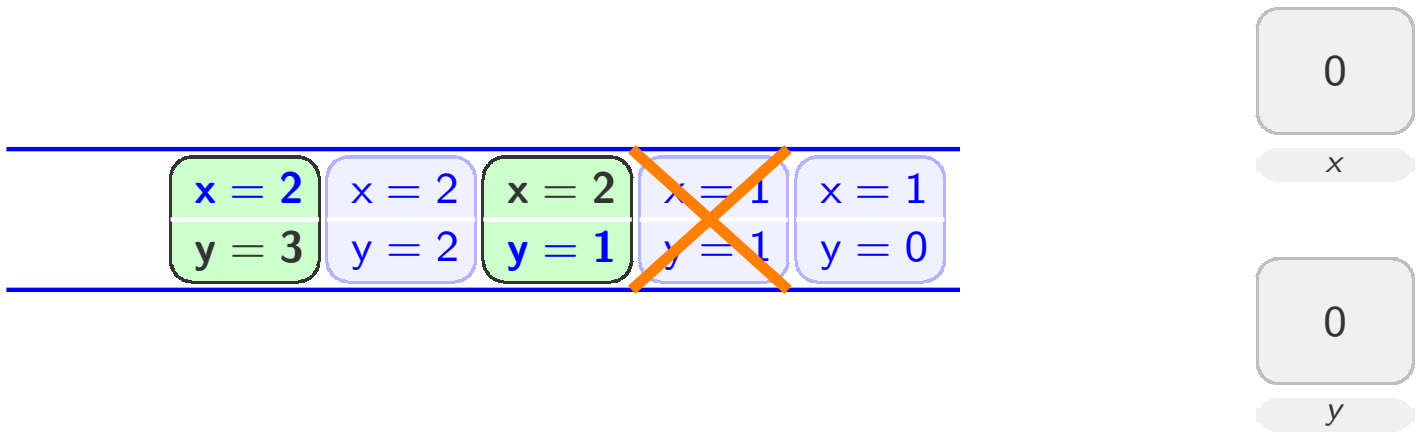

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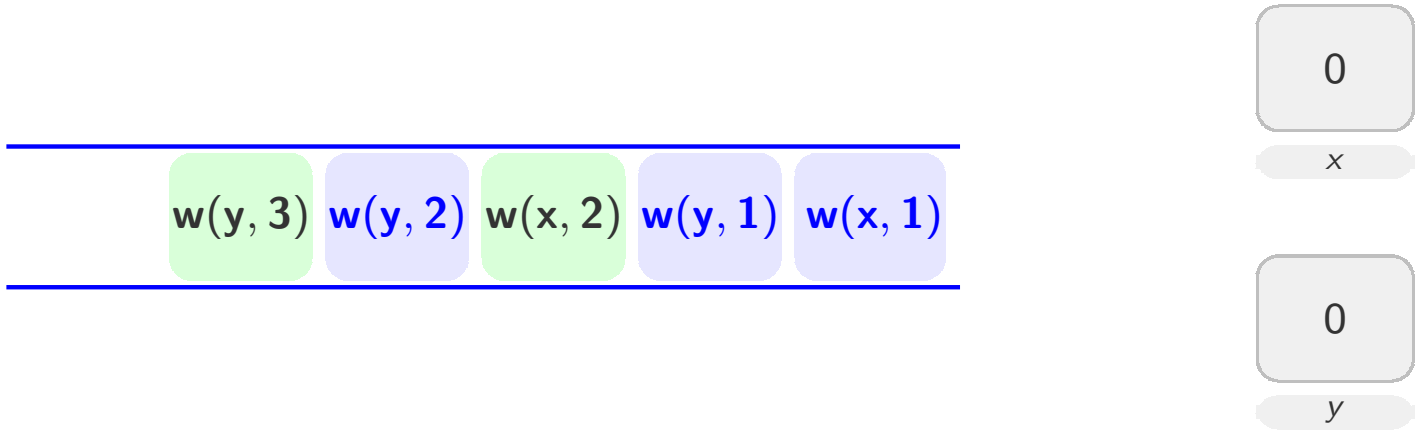

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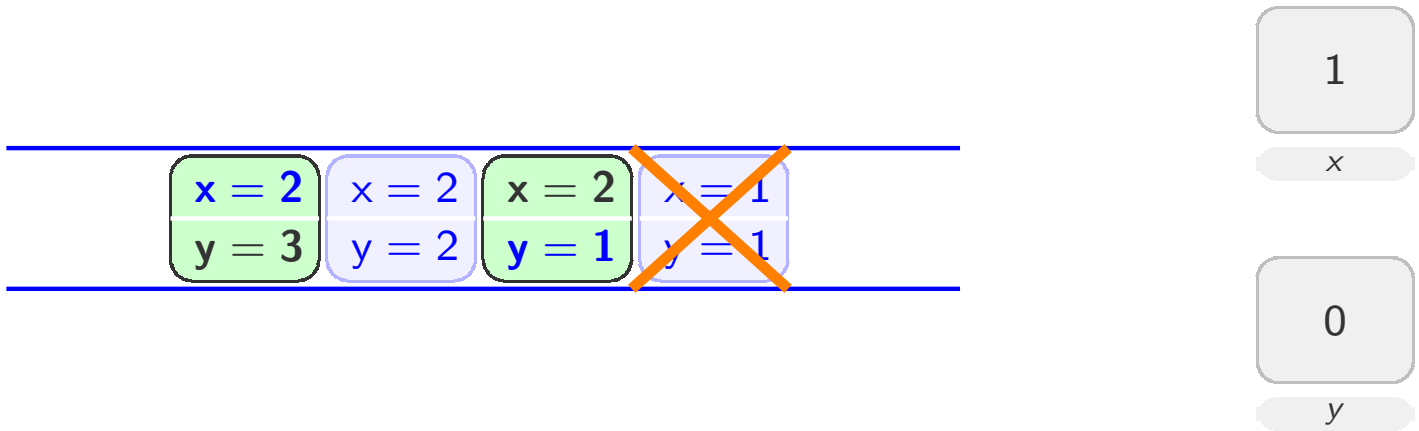

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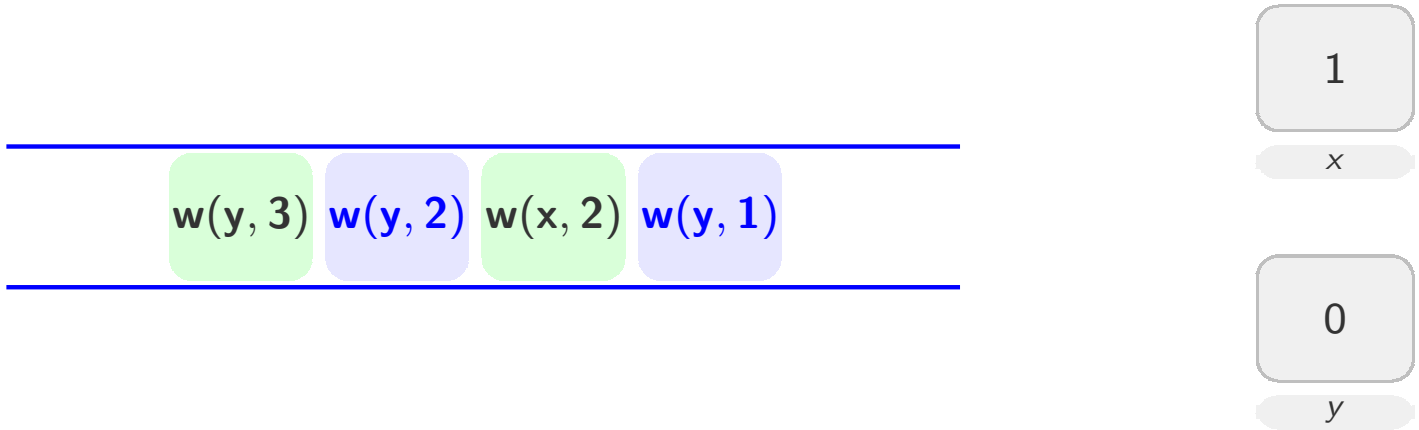
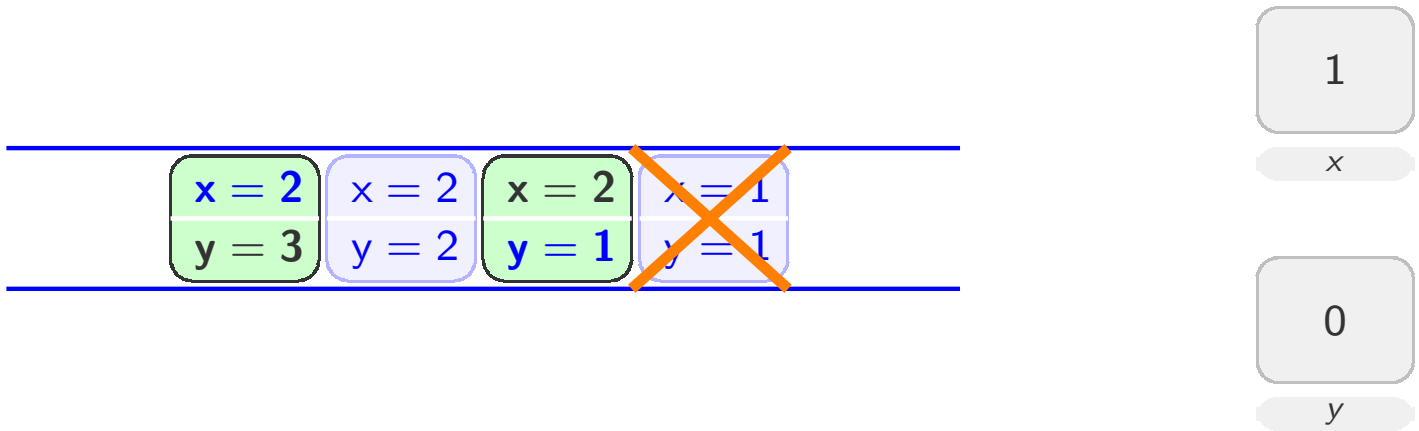


Channel= Sequence of memory states + Lossyness



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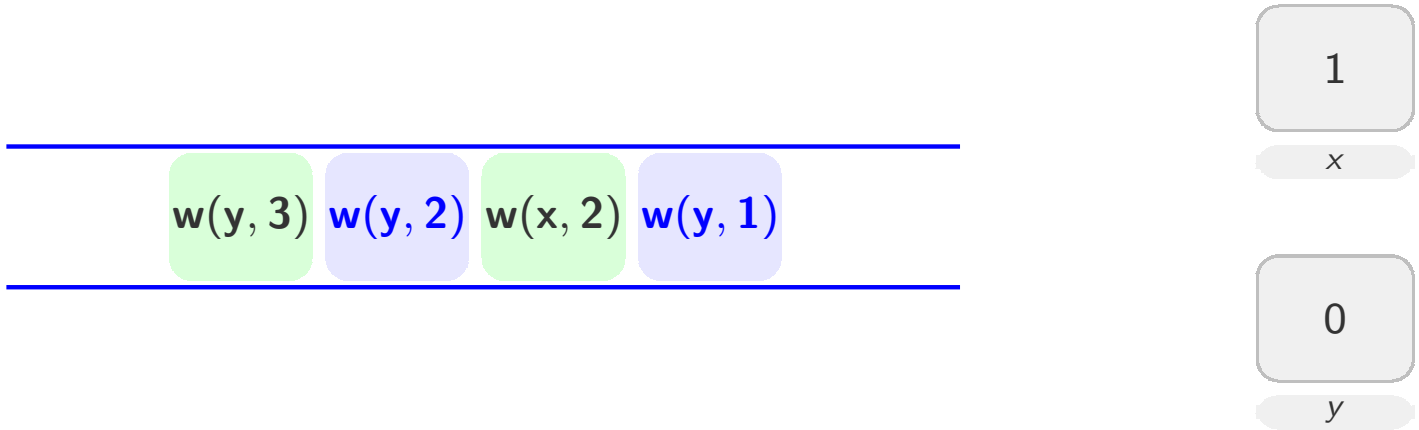

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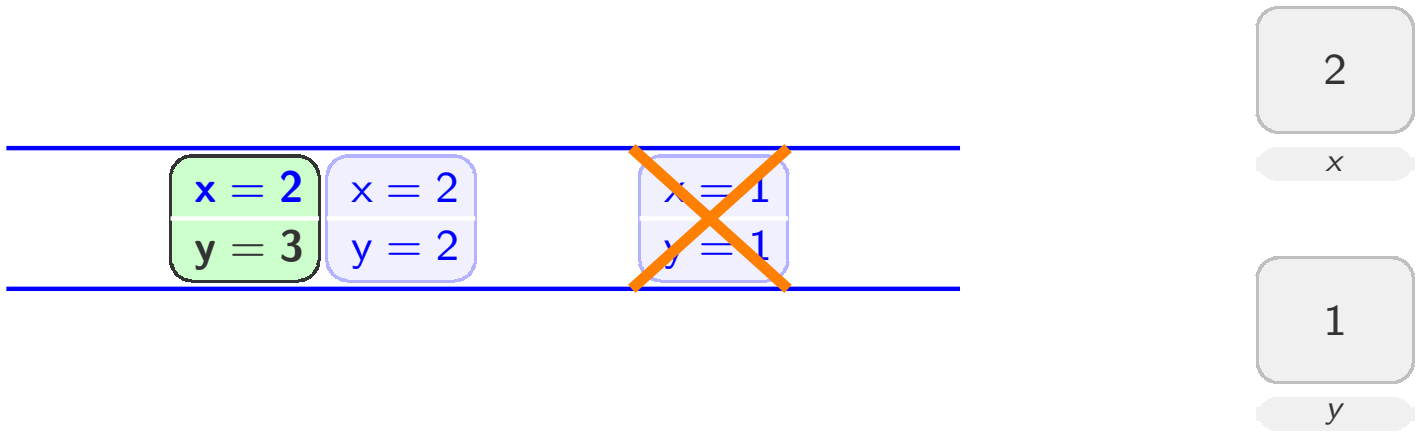

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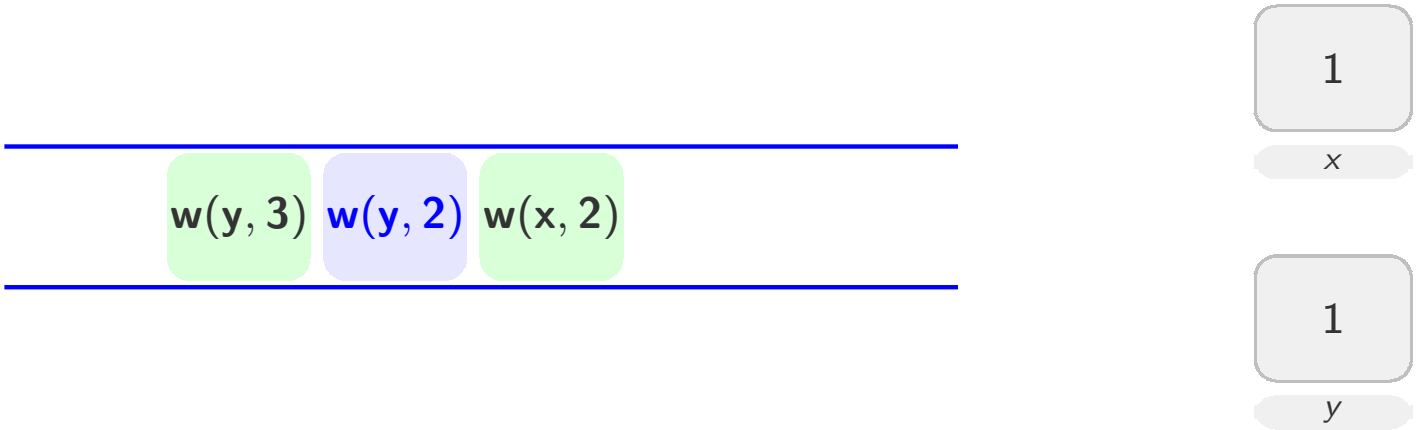

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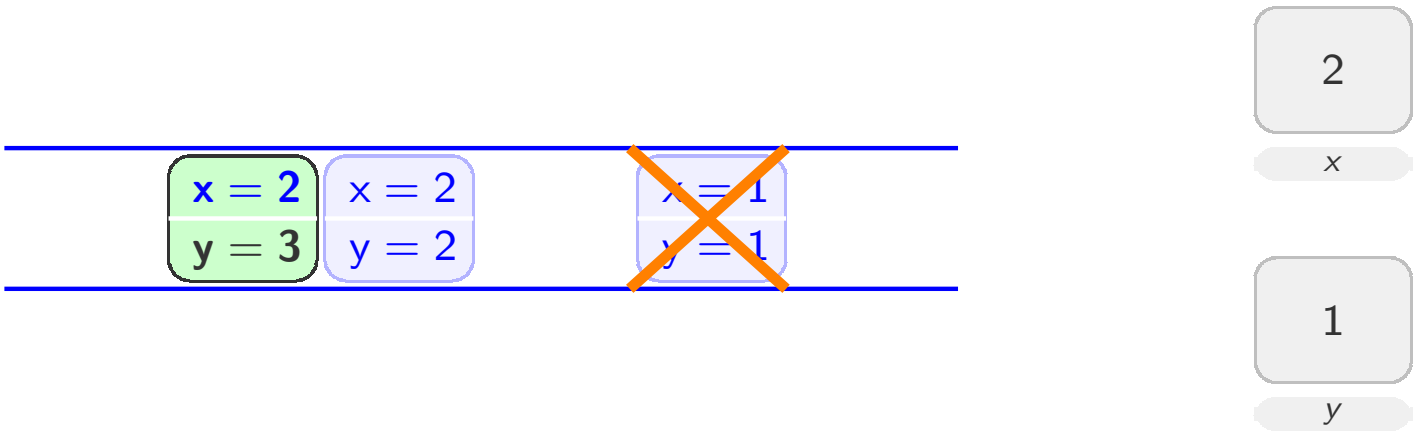

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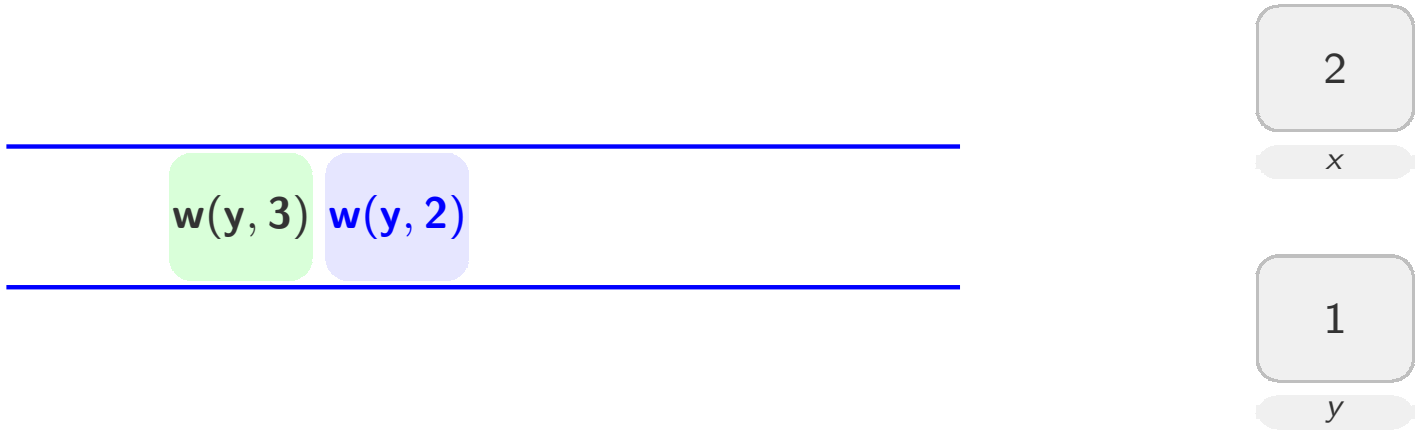

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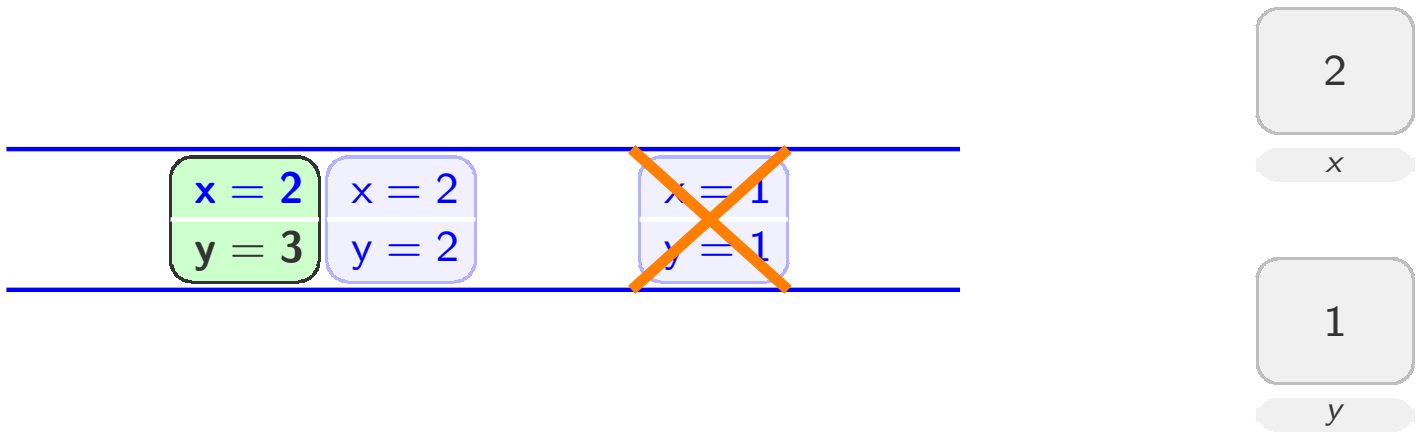

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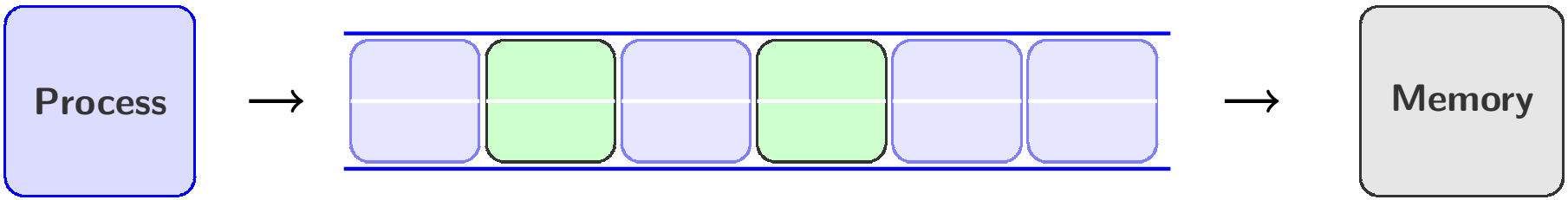

- *Write:* *Compute a new memory state; send it to the channel*
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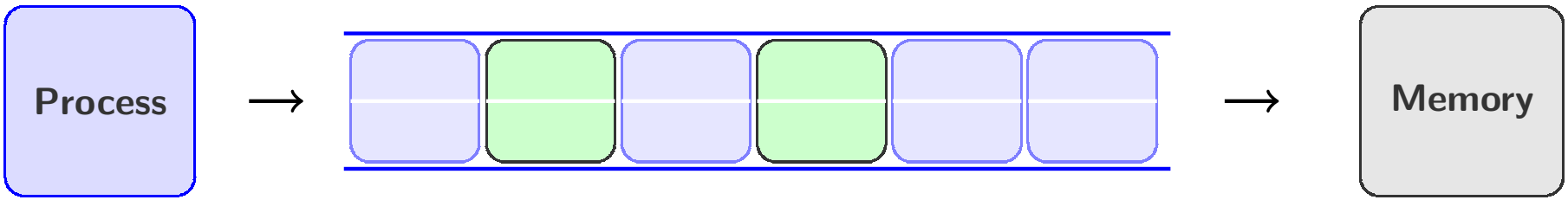
From W $\longrightarrow$ R systems to Lossy Channel Systems

- Problem: Interference between processes ?



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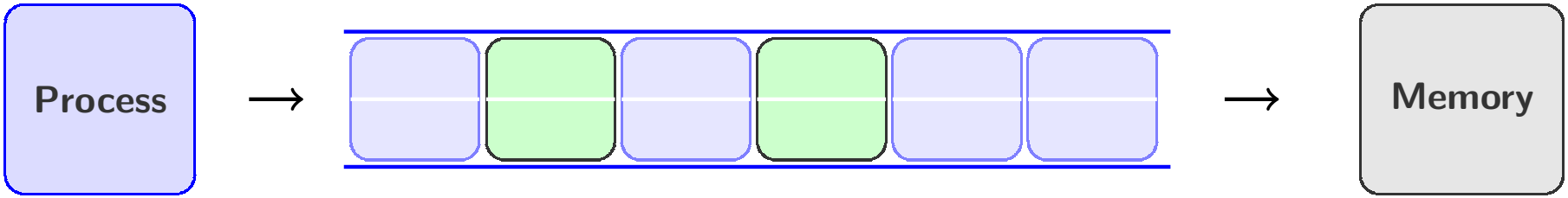

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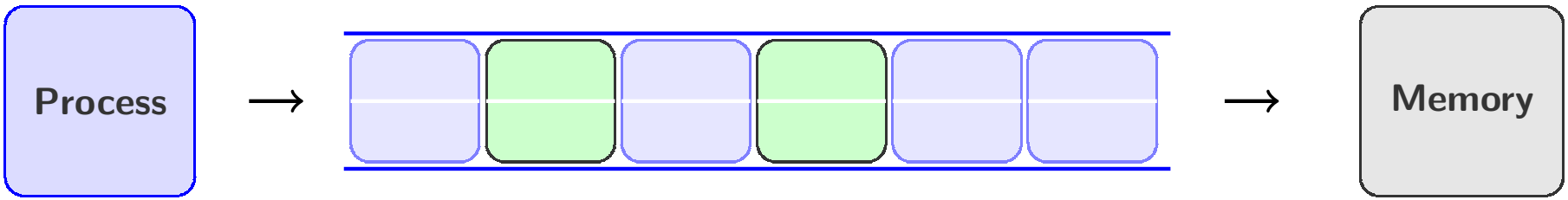

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  - *Memory update:* *Receive a state; copy it to the memory*
  - *Guessed Write:* *Send the guessed state to the channel*

- $\Rightarrow$ Check that all process agree on the sequence of states

  Synchronization of the lossy channel machines over send actions

Decidability for the State Reachability Problem

- Thm

  The state reachability problem for TSO (W $\rightarrow$ R) systems is reducible to the control-state reachability problem for LCS. The same holds for PSO (W $\rightarrow$ W/R) systems.

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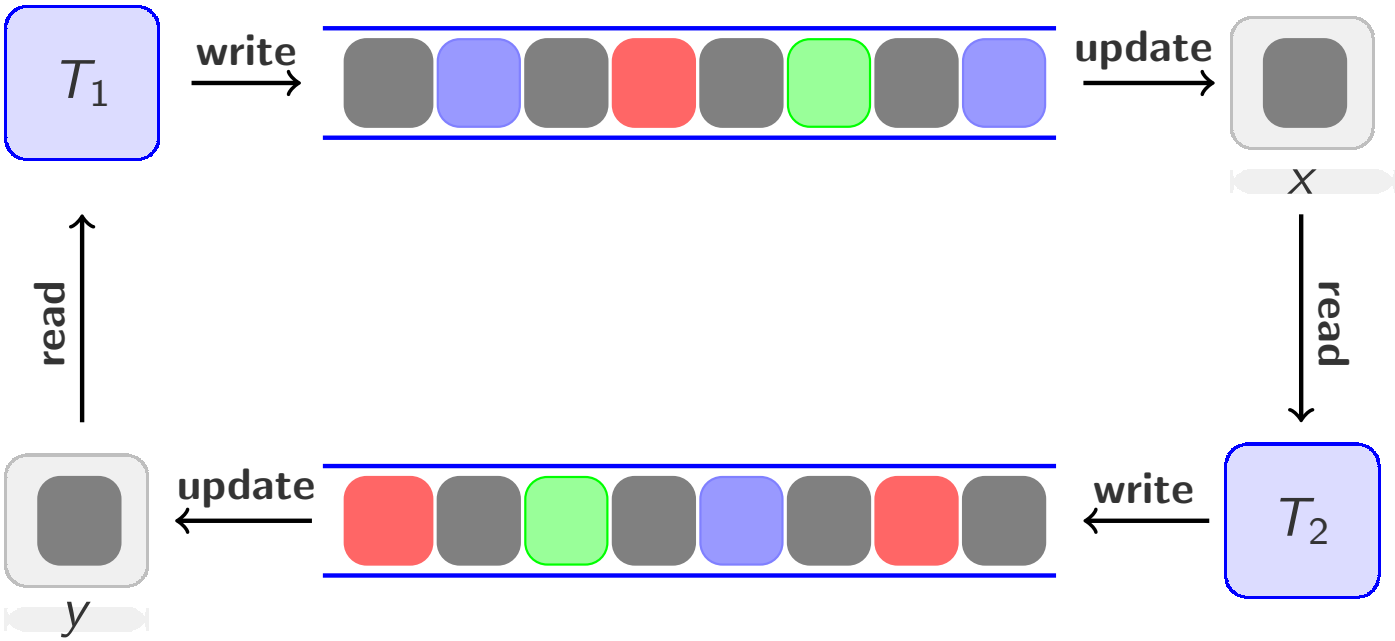
- Thm ([Abdulla, Jonsson, 1993])

  The control-state reachability problem for LCS is decidable

- Corollary

  The state reachability problem for TSO systems is decidable. The same holds for PSO systems.

From Lossy Channel Systems to W $\longrightarrow$ R systems



- T_1 simulates the lossy channel machine:
  - Send operation: Write operation of T_1 to the variable x
  - Read operation: Read operation of T_1 from the variable y
- T_2 transfers the successive values of the variable x to the variable y

Complexity / Undecidability results

- Thm

  Every LCS can be simulated by a TSO (W $\rightarrow$ R) system.
  The same holds for W $\rightarrow$ W/R *systems.*

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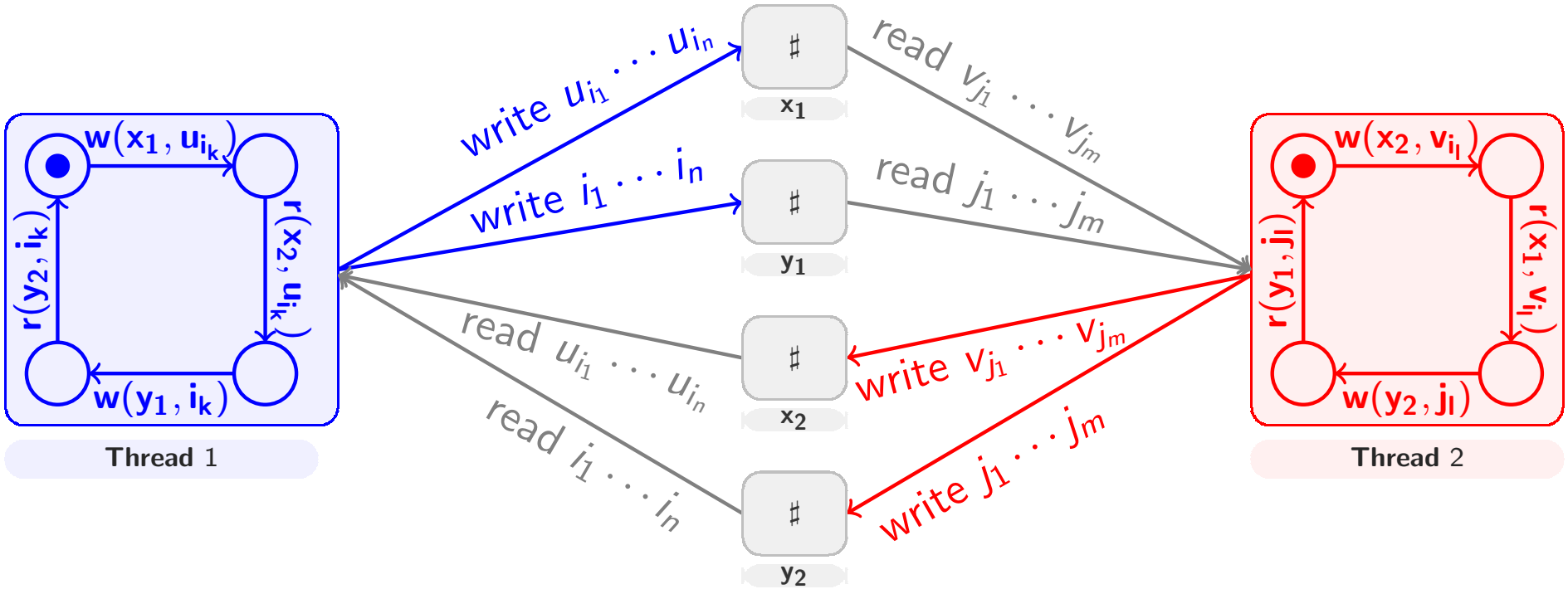
  The control-state reachability problem for LCS is nonprimitive recursive

- Thm ([Abdulla, Jonsson, 1993])

  The repeated control-state reachability problem for LCS is undecidable

$\Rightarrow$ Lower bound for the state RP, undec. for the repeated state RP.

From PCP to reachability in $WR \rightarrow WR$ systems



A solution for the reachability problem of the $WR \rightarrow WR$ system

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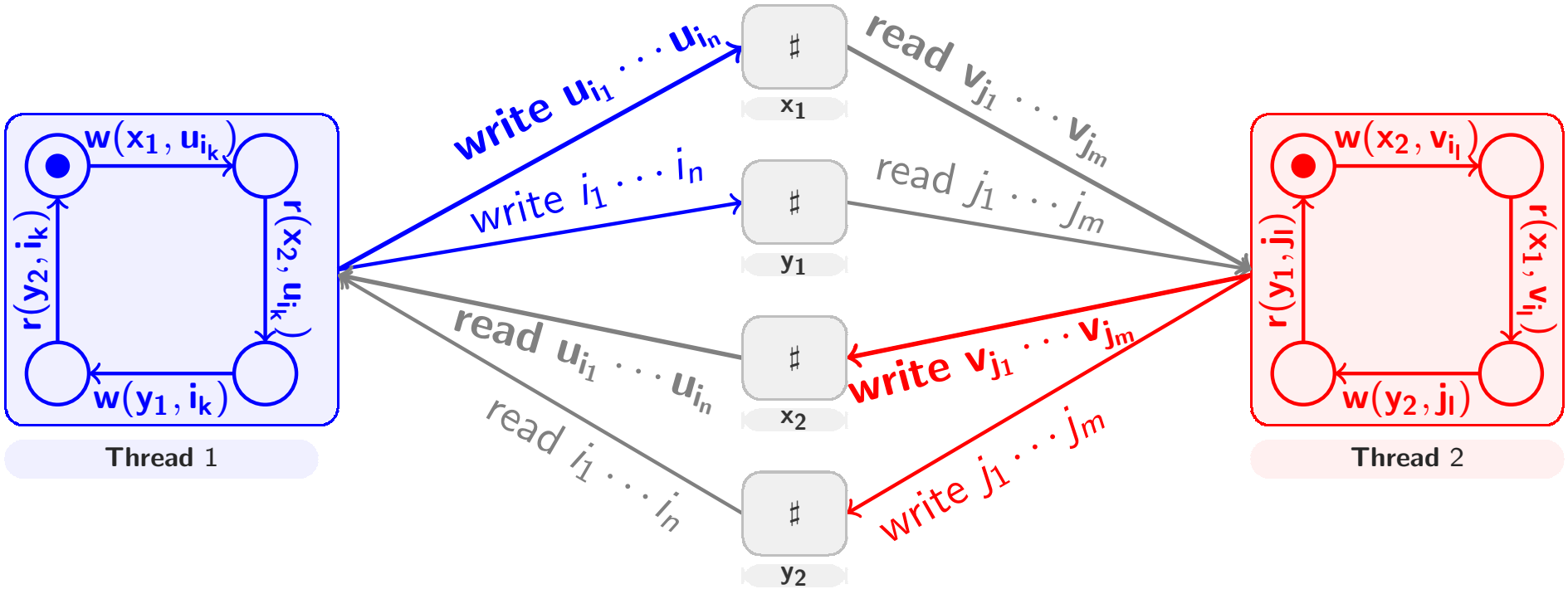

A solution for the reachability problem of the $WR \rightarrow WR$ system

$$u_{i_1} u_{i_2} \cdots u_{i_n} = v_{j_1} v_{j_2} \cdots v_{j_m}$$

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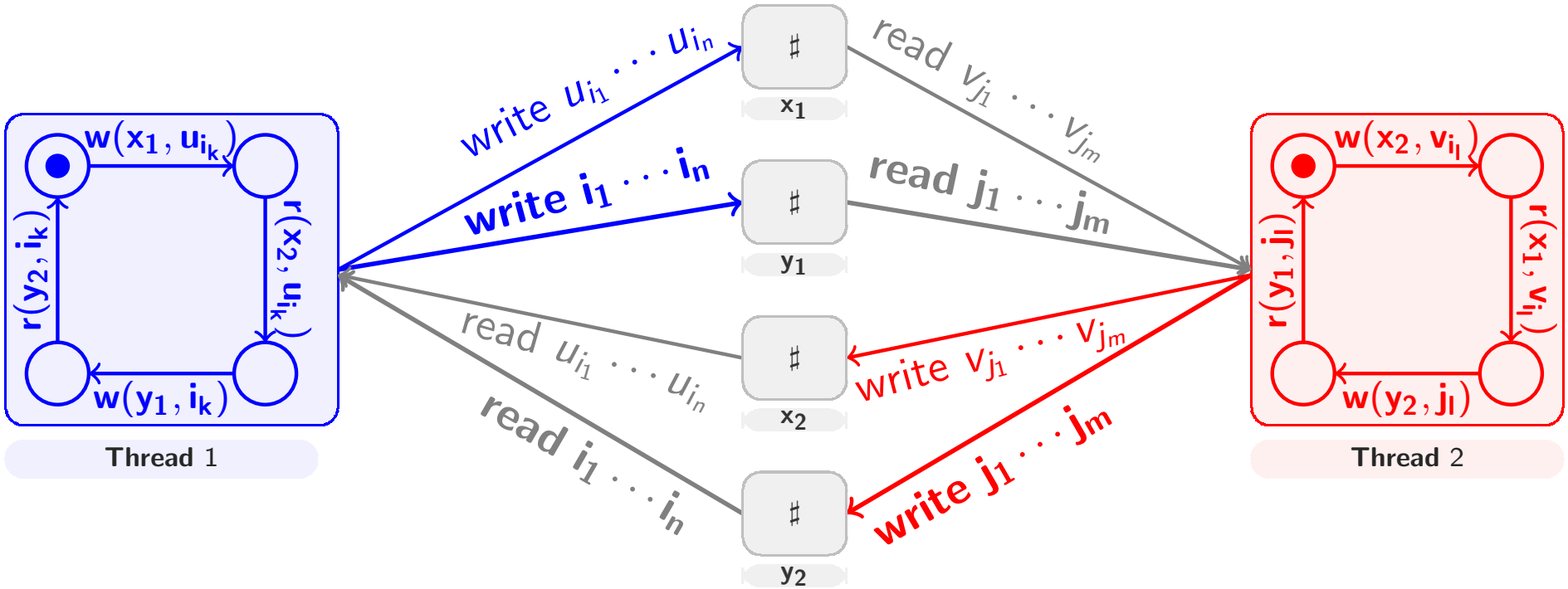

A solution for the reachability problem of the $WR \rightarrow WR$ system

$$u_{i_1} u_{i_2} \cdots u_{i_n} = v_{j_1} v_{j_2} \cdots v_{j_m} \text{ and } i_1 i_2 \cdots i_n = j_1 j_2 \cdots j_m$$

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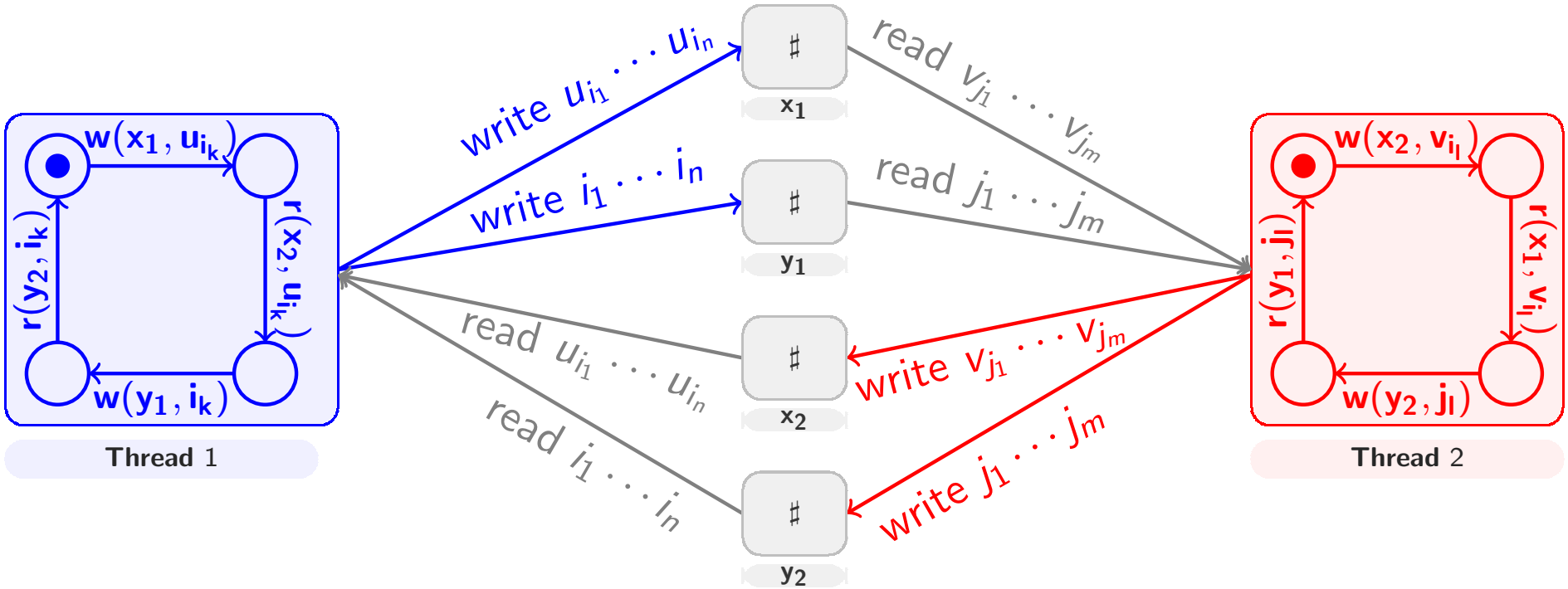

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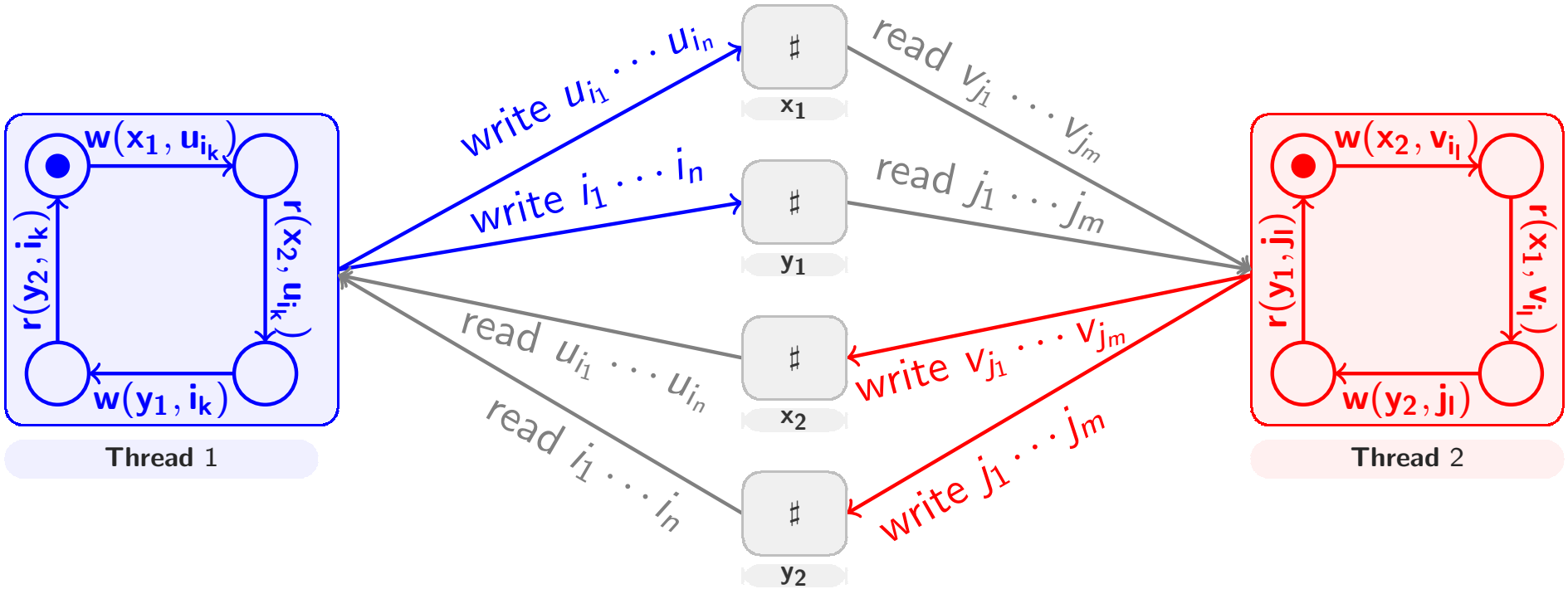
$\Rightarrow$ A solution for the Post Correspondence Problem

From PCP to reachability in $WR \rightarrow WR$ systems



Assume that: $u_{i_1} u_{i_2} \cdots u_{i_n} = v_{j_1} v_{j_2} \cdots v_{j_m}$ and $i_1 i_2 \cdots i_n = j_1 j_2 \cdots j_m$

T_1: $r(y_2, i_n)\ w(y_1, i_n)\ r(x_2, u_{i_n})\ w(x_1, u_{i_n}) \cdots r(y_2, i_1)\ w(y_1, i_1)\ r(x_2, u_{i_1})\ w(x_1, u_{i_1})$

T_2: $r(y_1, j_n)\ w(y_2, j_n)\ r(x_1, v_{j_n})\ w(x_2, v_{j_n}) \cdots r(y_1, j_1)\ w(y_2, j_1)\ r(x_1, v_{j_1})\ w(x_2, v_{j_1})$

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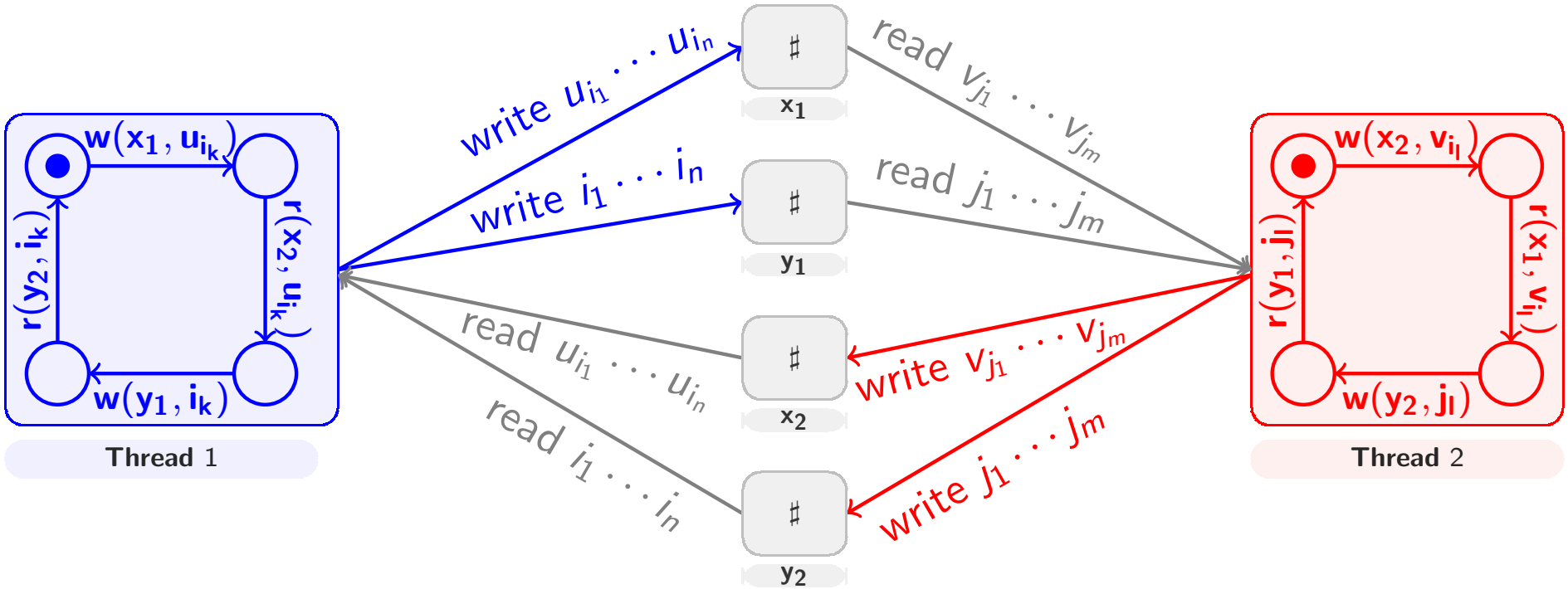

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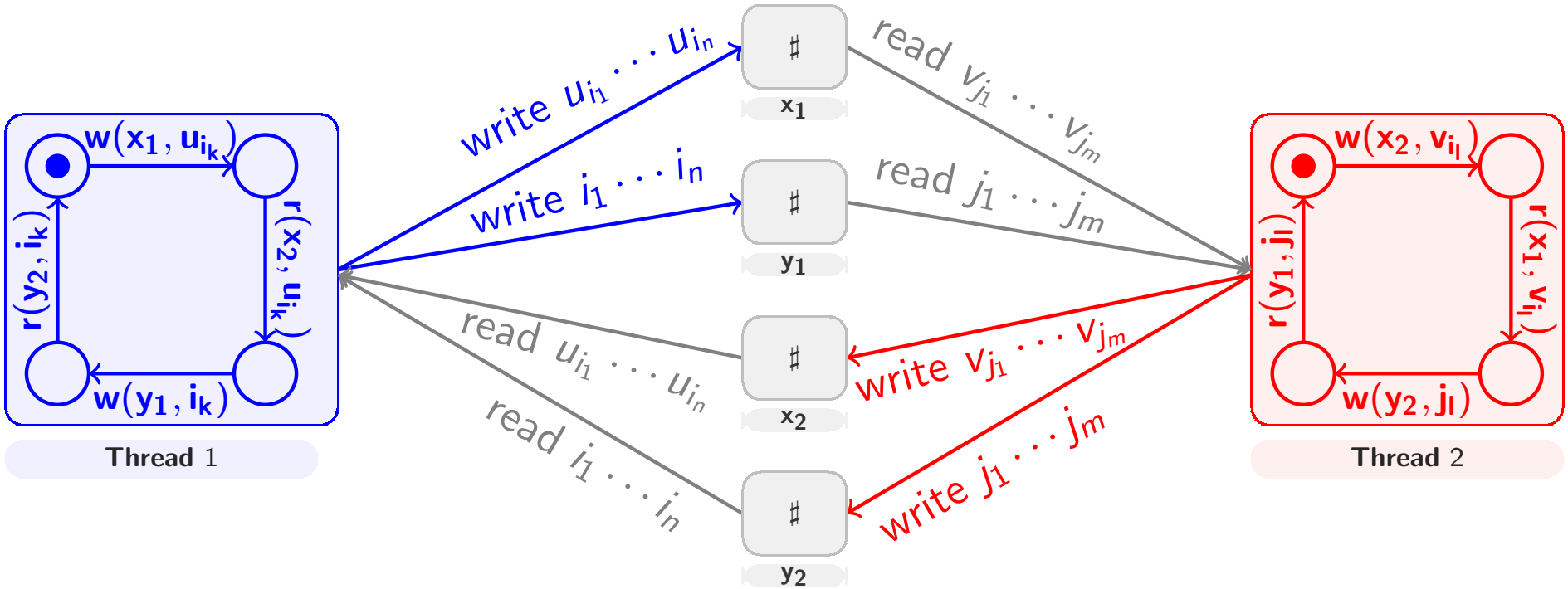

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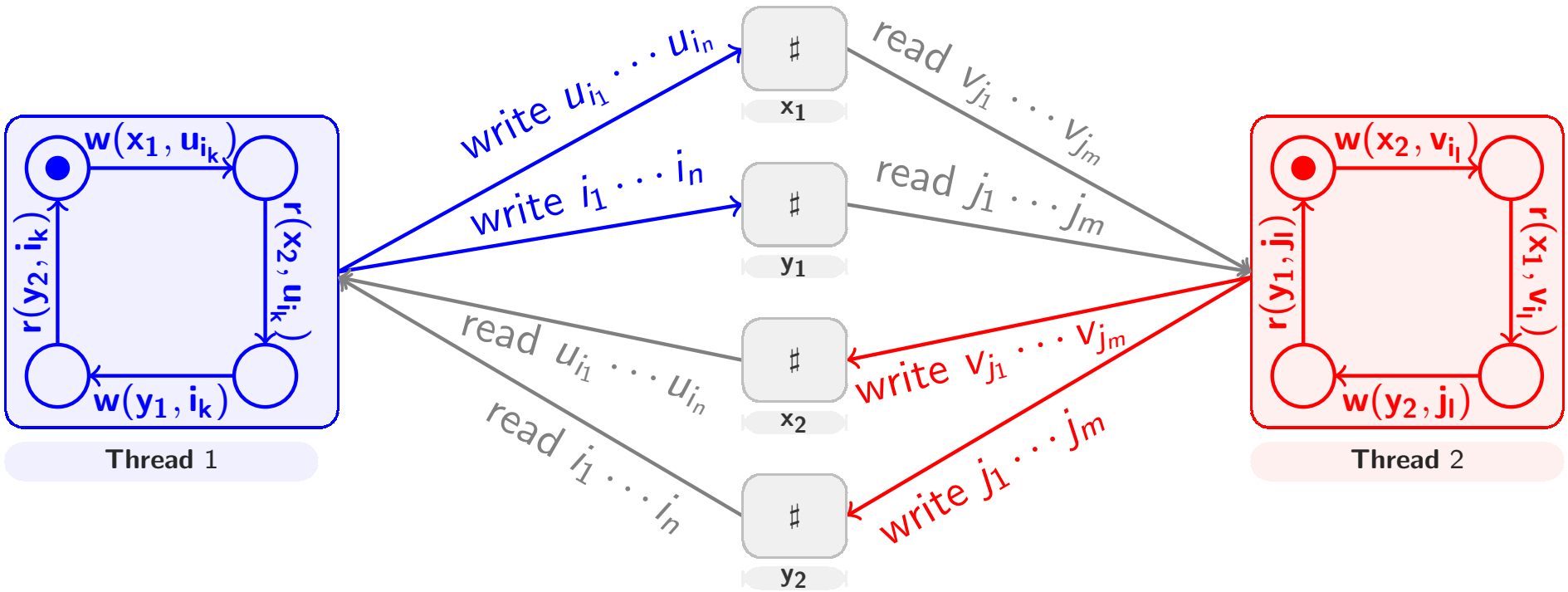
$\Rightarrow$ A solution for the reachability problem of the $WR \rightarrow WR$ system

From PCP to reachability in $(W \rightarrow R) + (R \rightarrow WR)$ systems



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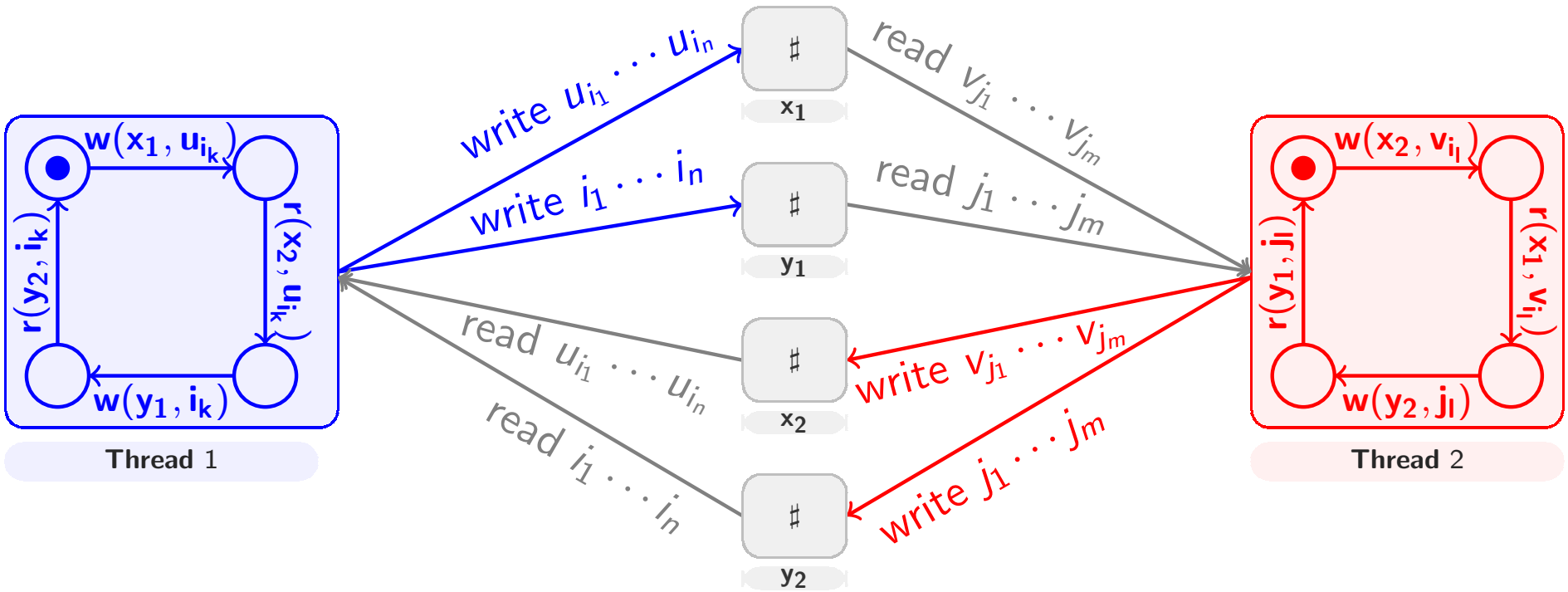

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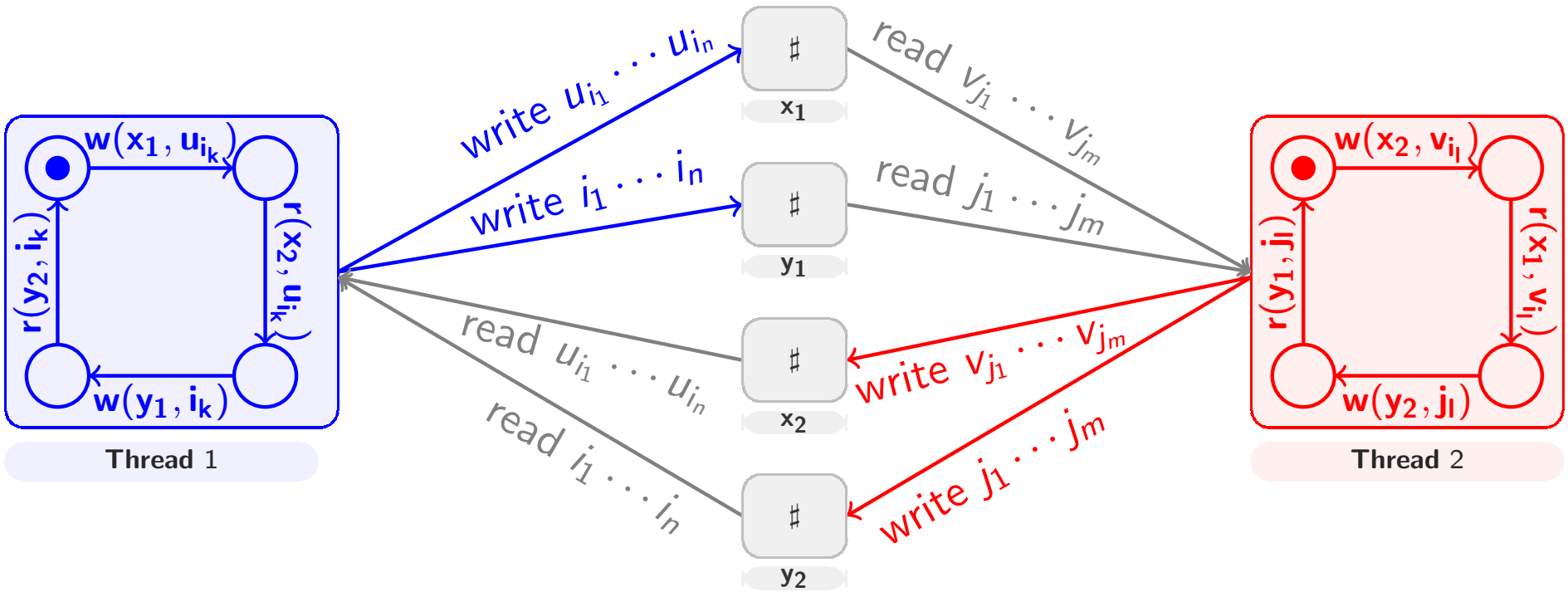

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$\Rightarrow$ Reachability in the $(W \rightarrow R) + (R \rightarrow RW)$ system

(Un)decidability results for WR $\rightarrow$ WR systems

- Thm

  PCP is reducible to state reachability in W/R $\rightarrow$ W/R *systems. The same holds for* (W $\rightarrow$ R) + (R $\rightarrow$ R/W) *systems.*

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- Thm

  State reachability in bounded-speculation W/R $\rightarrow$ W/R *systems is decidable.*
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Conclusion and future work

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- Fence insertion (make a program robust wrt SC)

Some work on WMM

- Adve and Gharachorloo,
  Shared Memory Consistency Models: A Tutorial, 1995
- S. Park, D. Dill,
  An executable specification, analyzer and verifier for RMO, 1995
- P. Chatterjee, G. Gopalakrishnan,
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- S. Sarkar, P. Sewell, F. Zappa Nardelli, S. Owens, T. Ridge, T. Braibant, M. O. Myreen, J. Alglave,
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- G. Boudol, G. Petri,
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