

# Logic Gates

## Digital Integrated Circuits

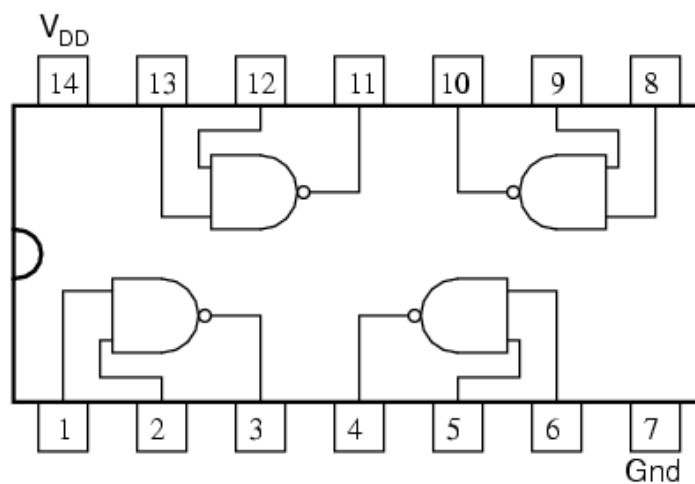
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### Aim

We use the Integrated Circuits to construct a logic circuit and verify the truth tables of AND/OR/NOT gates and their combinations.

### 1 Theory

*"Pinout," or "connection" diagram for the 4011 quad NAND gate*



I've used the schematic of a quad NAND gate as a representation to the kind of IC that I have used in the experiment which includes 7408 and 7432 corresponding to AND, and OR respectively. The NOT gate IC (7404) is different in that it has 6 NOT gates in it.

Digital logic circuitry does not make use of split power supplies as op-amps do. Like op-amp circuits, though, ground is still the implicit point of reference for all voltage measurements. If we were to speak of a "high" signal being present on a certain pin of the chip, I would mean that there

was full voltage between that pin and the negative side of the power supply (ground).

WE can describe a digital circuit as follows. They deal with signals restricted to the extreme limits of zero and some full amount. This stands in contrast to analog circuits, in which signals are free to vary continuously between the limits imposed by power supply voltage and circuit resistances. These circuits find use in "true/false" logical operations and digital computation.

## 2 Procedure and Results

We get to familiarize with the circuit even though a thorough familiarization with the actual circuit inside the IC is not so easy. The basic circuit for all the gates is the same. We supply a power supply through the pins 7 and 14 of the IC where the positive lead from the DC voltage supply goes to 14 and pin 7 is grounded (effectively connected to the negative terminal). As we can see in the above schematic diagram, we connect the schematic input leads of the gates (i.e. like pins 1 and 2) to the ground line via switches. Now, by varying the switch position we can get an output from the pin 3 which can be measured using a DMM. Basic principle that we are relying on here is that, when 0V is applied, the amplifier is cut-off and the output is the plate voltage ( $V_{CC}$ ), i.e. it is high. When positive voltage is applied, it drives the collector voltage to the logic low voltage.

### 2.1 AND Gate (7408)

S.No	Switch 1 pos.	Switch 2 pos.	Voltage at pin 3 (V)	Gate output
1	0	0	0.160	0
2	0	1	0.160	0
3	1	0	0.160	0
4	1	1	4.63	1

This is the expected truth table of an AND gate. The residue voltages which are considered as zeroes can be interpreted as the plate voltage.

### 2.2 OR Gate (7432)

S.No	Switch 1 pos.	Switch 2 pos.	Voltage at pin 3 (V)	Gate output
1	0	0	0.142	0
2	0	1	4.63	1
3	1	0	4.63	1
4	1	1	4.63	1

### 2.3 NOT Gate (7404)

NOT gate reverses the input if the switch is on.

S.No	Switch 1 pos.	Voltage at pin 2 (V)	Gate output
1	0	4.65	1
2	1	0.161	0

Now, let's look at some combination of gates.

### 2.4 AND Gate combines with OR Gate

We have two possible combinations where in one case we take the output from the AND gate and give it as one of the inputs for the OR gate and the vice-versa. Here, we have three switches in total; two in the first gate and one in the second gate. Let's look at both of them.

#### 2.4.1 Output from AND taken as input of OR

S.No	Switch 1 pos.	Switch 2 pos.	Switch 3 pos	V at pin 3 of OR Gate(V)	Gate output
1	0	0	0	0.142	0
2	0	0	1	4.63	1
3	0	1	0	0.142	0
4	1	0	0	0.142	0
5	0	1	1	4.63	1
6	1	0	1	4.63	1
7	1	1	0	4.63	1
8	1	1	1	4.63	1

#### 2.4.2 Output from OR taken as input of AND

S.No	Switch 1 pos.	Switch 2 pos.	Switch 3 pos	V at pin 3 of AND Gate(V)	Gate output
1	0	0	0	0.160	0
2	0	0	1	0.160	0
3	0	1	0	0.160	0
4	1	0	0	0.160	0
5	0	1	1	4.68	1
6	1	0	1	4.68	1
7	1	1	0	0.160	0
8	1	1	1	4.68	1

We can see from this very clearly that AND(OR) is not same as OR(AND).

## 2.5 combination of NOT and OR gates

Similar to the above case, here also we have 2 possibilities i.e. NOT(OR) and OR(NOT) where NOT(OR) is also known as the NOR gate. Here, there are only two switches as there is only one input to a NOT gate.

### 2.5.1 NOR Gate

S.No	Switch 1 pos.	Switch 2 pos.	V at pin 2 of NOT Gate(V)	Gate output
1	0	0	4.65	1
2	0	1	0.161	0
3	1	0	0.161	0
4	1	1	0.161	0

This is what we expect from a NOT gate as it reverses whatever the TRUTH table of OR gate is.

### 2.5.2 Output of NOT Gate as input to OR Gate

S.No	Switch 1 pos.	Switch 2 pos.	V at pin 3 of OR Gate(V)	Gate output
1	0	0	4.63	1
2	0	1	4.63	1
3	1	0	0.143	0
4	1	1	4.63	1

## 2.6 Combination of NOT and AND gates

Same as in the previous case we have NOT(AND) and AND(NOT) where NOT(AND) is also known as NAND gate. Let's look at the truth table output.

### 2.6.1 NAND Gate

S.No	Switch 1 pos.	Switch 2 pos.	V at pin 2 of NOT Gate(V)	Gate output
1	0	0	4.68	1
2	0	1	4.68	1
3	1	0	4.68	1
4	1	1	0.142	0

NAND gate is the reverse of AND Gate, hence the above truth table is the expected one.

**2.6.2 Output from NOT given as input to AND**

S.No	Switch 1 pos.	Switch 2 pos.	V at pin 3 of AND Gate(V)	Gate output
1	0	0	0.464	0
2	0	1	4.99	1
3	1	0	0.464	0
4	1	1	0.464	0

**2.7 Three gate combination  $OR(NOT(AND)) \equiv OR(NAND)$ .**

S.No	Switch 1 pos.	Switch 2 pos.	Switch 3 pos	V at pin 3 of OR Gate(V)	Gate output
1	0	0	0	4.63	1
2	0	0	1	4.63	1
3	0	1	0	4.63	1
4	1	0	0	4.63	1
5	0	1	1	4.63	1
6	1	0	1	4.63	1
7	1	1	0	0.143	0
8	1	1	1	4.63	1