A Note on Depth Reduction: A Simple Proof of the Chasm

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Abstract

Agrawal and Vinay [AV08] showed how any subexponential arithmetic circuit can be thought of as a depth four subexponential arithmetic circuit. This unexpected depth reduction to constant depth is in contrast to curcuits in the Boolean setting. The resulting circuit size in this simulation was more carefully analyzed by Korian [Koi12] and subsequently by Tavenas [Tav13]. We provide a simple proof of this chain of results. We then abstract the main ingredient to apply it to formulas and constant depth circuits.

1 Introduction

Agrawal and Vinay [AV08] showed how any subexponential arithmetic circuit can be thought of as a depth four subexponential arithmetic circuit. This provided a new direction to seek lower bounds in arithmetic circuits. A long list of papers attest to increasingly sophisticated lower bound arguments, centered around the idea of shifted partial derivates due to Kayal, to separate the so called arithmetic version of P vs NP. See for example, this non-exhaustive list [Kay12, GKKS13, KSS14, FLMS14, KS14b, KLSS14, KS14c, KS14a].

The depth reduction chasm was more carefully analyzed by Korian [Koi12] and subsequently by Tavenas [Tav13]. Given the importance of these depth reduction chasms, it is natural to seek new and/or simpler proofs. We do just that.

We use a simple combinatorial property to prove our result. We then show how this can be extended to showing chasms for formulas and constant depth circuits. In the case of formulas, we show the top layer of multiplication gates have a much larger number of factors and therefore has more structure than a typical depth reduced circuit. We hope that such structural properties lead to better lower bounds for formulas.

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2 Reduction to depth four circuits

We shall need the classical depth reduction of [VSBR83, AJMV98].

Theorem 1 ([VSBR83, AJMV98]). *Let f be an n-variate degree d polynomial computed by an arithmetic circuit Φ of size s. Then there is an arithmetic circuit Φ' computing f and has size $s' = \mathsf{poly}(s, n, d)$ and depth $O(\log d)$.*

Moreover, the reduced circuit Φ' has the following properties:

1. The circuit is homogeneous.
2. All multiplication gates have fan-in at most 5.
3. If u is any multiplication gate of Φ', all its children v satisfy $\deg(v) \leq \deg(u)/2$.

These properties can be inferred from their proof. A simple self-contained proof may be seen in [Sap15, Chapter 5]

Agrawal and Vinay [AV08] showed that arithmetic circuits can in fact be reduced to depth four, and the result was subsequently strengthened by Koiran [Koi12] and by Tavenas [Tav13].

Theorem 2 ([AV08, Koi12, Tav13]). *Let f be an n-variate degree d polynomial computed by a size s arithmetic circuit. Then, for any $0 < t \leq d$, f can be computed by a homogeneous $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit of top fan-in $s^{O(d/t)}$ and size $s^{O(t+d/t)}$.*

To optimize the size of the final depth four circuit, we should choose $t = \sqrt{d}$ to get a $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit of size $s^{O(\sqrt{d})}$. Note that this implies that if we could prove a lower bound of $n^{\omega(\sqrt{d})}$ for such $\Sigma\Pi\Sigma\Pi^{[\sqrt{d}]}$ circuits, then we would have proved a lower bound for general circuits. In this section, we shall see a simple proof of Theorem 2.

Proof of Theorem 2. Let C be the $O(\log d)$ depth circuit computing f obtained from Theorem 1 applied on the size s circuit computing f. Let s' be the size of C. If g is a polynomial computed at any intermediate node of C, then from the structure of C we have a homogeneous expression

$$g \quad = \quad \sum_{i=1}^{s'} g_{i1} \cdot g_{i2} \cdot g_{i3} \cdot g_{i4} \cdot g_{i5} \tag{3}$$

where each g_{ij} is computed by a node in C as well, and $\deg(g_{ij}) \leq \deg(g)/2$. In particular, if g were the output gate of the circuit, the RHS may be interpreted as a $\Sigma\Pi\Sigma\Pi^{[d/2]}$ circuit of top fan-in s' computing f. To obtain a $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit eventually, we shall perform the following steps on the output gate:

1. For each summand $g_{i1} \dots g_{ir}$ in the RHS, pick the gate g_{ij} with largest degree (if there is a tie, pick the one with smaller index j). If g_{ij} has degree greater than t, expand g_{ij} in-place using (3).
2. Repeat this process until all g_{ij}'s on the RHS have degree at most t.

Each iteration of the above procedure increases the top fan-in by a multiplicative factor of s'. If we could show that the in $O(d/t)$ iterations all terms on the RHS have degree at most t, then we would have obtained an $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit of top fanin $s'^{O(d/t)}$ computing f.

Label a term *bad* in its degree is more than $t/8$. To bound the number of iterations, we count the number of bad terms in each summand. Since we would always maintain homogeneity, the number of bad terms in any summand is at most $8d/t$ (i.e., not too many). We show each iteration *increases* the number of bad terms by at least one. This bounds the number of iterations by $8d/t$.

In (3), if $\deg(g) = k$, the largest degree term of any summand on the RHS is at least $k/5$ (since the sum of the degrees of the five terms must add up to k) and so continues to be bad. But the largest degree term can have degree at most $k/2$. Hence the other four terms must together contribute at least $k/2$ to the degree. This implies that the second largest term in each summand has degree at least $k/8$. This term is bad too, if we started with a term of degree greater than t. Therefore, as long as we are expanding terms of degree more than t using (3), we are guaranteed its replacements have at least one additional bad term. As argued earlier, we can never have more than $8d/t$ such terms in any summand and this bounds the number of iterations by $8d/t$.

When the above procedure stops, we have an $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit of top fan-in $s'^{O(8d/t)} = s^{O(d/t)}$. Since a polynomial of degree t can have at most n^t monomials, the overall size of the circuit is at most $s^{O(t+d/t)}$. □

3 Depth reduction for homogeneous formulas

For the class of homogeneous formulas and shallow circuits, we will show that they can be depth reduced to a more structured depth four circuit.

To quickly recap the earlier proof, we began with an equation $f = \sum_i g_{i1} \cdot g_{i2} \cdot g_{i3} \cdot g_{i4} \cdot g_{i5}$ and recursively applied the same expansion on all the large degree g_{ij}'s. The only property we really used was that in the above equation, there were at least two g_{ij} that had large degree.

For the case of homogeneous formulas and shallow circuits, there are better expansions that we could use as a starting point.

Theorem 4 ([HY11])**.** *Let f be an n-variate degree d polynomial computed by a size s homogeneous formula. Then, f can be expressed as*

$$f \quad = \quad \sum_{i=1}^{s} f_{i1} \cdot f_{i2} \cdots f_{ir} \tag{5}$$

where

1. *the expression is homogeneous,*
2. *for each i, j, we have $\left(\frac{1}{3}\right)^j d \leq \deg(f_{ij}) \leq \left(\frac{2}{3}\right)^j d$ and $r = \Theta(\log d)$,*

3. *each f_{ij} is also computed by homogeneous formulas of size at most s.*

With this, we are ready to prove a more structured depth reduction for homogeneous formulas.

Theorem 6. *Let f be an n-variate degree d polynomial computed by a size s homogeneous formula. Then for any parameter $t = o(d)$, we can compute f equivalently by a homogeneous $\Sigma\Pi^{[\Theta((d/t)\log t)]}\Sigma\Pi^{[t]}$ circuit of top fan-in at most $s^{O(d/t)}$ and size $s^{O(t+d/t)}$.*

The resulting depth four circuit is more structured in the sense that the multiplication gates at the second layer have a much larger fan-in (by a factor of $\log t$). In Theorem 2, we only know that the polynomials feeding into these multiplication gates have degree at most t. The theorem above states that if we were to begin with a homogeneous formula, the degree t polynomials factorize further to give $\Theta((d/t)\log t)$ non-trivial polynomials instead of $\Theta(d/t)$ as obtained in Theorem 2.

Proof. We start with equation (5) which is easily seen to be a homogeneous $\Sigma\Pi\Sigma\Pi^{[2d/3]}$ circuit with top fan-in s:

$$f \quad = \quad \sum_{i=1}^{s} f_{i1} \cdot f_{i2} \cdots f_{ir}$$

To obtain a $\Sigma\Pi^{[\Theta((d/t)\log t)]}\Sigma\Pi^{[t]}$ circuit eventually, we shall perform the following steps on the output gate:

1. For each summand $f_{i1} \ldots f_{ir}$ in the RHS, pick the gate f_{ij} with largest degree (if there is a tie, pick the one with smaller index j). If f_{ij} has degree more than t, expand that f_{ij} in-place using (5).
2. Repeat this process until all f_{ij}'s on the RHS have degree at most t.

Each iteration again increases the top fan-in by a factor of s. Again, as long as we are expanding terms using (5) of degree $k > t$, we are guaranteed by Theorem 4 that each new summand has at least one more term of degree at least $k/9 > t/9$. Thus, the number of iterations must be bounded by $9d/t$ thereby yielding a $\Sigma\Pi\Sigma\Pi^{[t]}$ of top fan-in at most $s^{O(d/t)}$ and size $s^{O(t+d/t)}$.

We shall now show that we require $\Theta(d/t)$ iterations to make all the terms have degree at most t. We will say a term is *small* if degree is at most t and *big* otherwise. To prove a lower bound on the number of iterations, we shall use a different potential function — the total degree of all the big terms.

Given the geometric progression of degrees in Theorem 4, we see that the total degree of all the small terms in any summand is bounded above by $2t$. Hence, the total degree of all the big terms is $d - O(t) = O(d)$ since $t = o(d)$. But whenever (5) is applied on a big term, we introduce several small degree terms with total degree $2t$. Hence, the total degree of all big terms reduce by at most $2t$ additively. This implies that we require $\Omega(d/t)$ iterations to make it constant.

Since every expansion via (5) introduces at least $\Theta(\log t)$ non-trivial terms, it would then follow that every summand at the end has $\Omega((d/t)\log t)$ non-trivial factors. □

3.1 An alternate proof

While we proved Theorem 6 along the lines of Theorem 2, it is possible to provide an alternate proof of it. We provide a sketch. Starting with a homogeneous formula, by Theorem 2 we get a $\Sigma\Pi\Sigma\Pi^{[t]}$ circuit of the form

$$\sum_{i=1}^{s'} Q_{i1} \cdots Q_{ir}$$

where $\deg(Q_{ij}) \leq t$ and $s' = s^{O(d/t)}$. From the innards of this proof, you can convince yourself that each of the Q_{ij}'s is indeed computable by a homogeneous formula (formula, not a circuit) of size at most s. By multiplying several polynomials (if necessary) of degree at most $t/2$, we may assume that there are $\Theta(d/t)$ polynomials Q_{ij} in each summand, with their degree between $t/2$ and t.

Each of these polynomials may be expanded using (5). Since each such expansion adds $O(\log t)$ additional factors and increases the fan-in by a factor of s, the overall top fan-in is now $s' \cdot s^{O(d/t)}$. The number of factors however increases from $\Theta(d/t)$ to $\Theta((d/t)\log t)$. The resulting circuit is thus a $\Sigma\Pi^{[\Theta((d/t)\log t)]}\Sigma\Pi^{[t]}$ circuit of top fan-in $s^{O(d/t)}$.

4 Depth reduction on constant depth circuits

In the same vein, a natural question is if we can obtain more structure for a constant depth circuit. For example, is the resulting depth four circuit more structured when we begin with a depth 100 circuit? By suitably adapting the expansion equation, our approach can answer this question.

Lemma 7. *Let f be an n-variate degree d polynomial computed by a size s circuit of product-depth*[1] *Δ. Then f can be expressed as*

$$f \quad = \quad \sum_{i=1}^{s^2} f_{i2} \cdot f_{i3} \cdots f_{ir} \ \cdot \ g_{i1} \cdots g_{i\ell} \tag{8}$$

where

1. *the expression is homogeneous,*
2. *for each i, j, we have $\left(\frac{1}{3}\right)^j d \leq \deg(f_{ij}) \leq \left(\frac{2}{3}\right)^j d$ and $r = \Theta(\log d)$,*
3. *each f_{ij} and g_{ij} is also computed by homogeneous formulas of size at most s and product-depth Δ.*
4. *$\ell = \Omega(d^{1/\Delta})$*

[1] the product depth is the number of multiplication gates encountered in any path from root to leaf

5. *all g_{ij}, f_{ij} are polynomials of degree at least* 1.

Using this equation for the depth reduction yields the following theorem.

Theorem 9. *Let f be an n-variate degree d polynomial computed by a size s homogeneous formula of product-depth Δ. Then for any parameter $t = o(d)$, we can compute f equivalently by a homogeneous $\Sigma\Pi^{[\Theta((d/t)\cdot t^{1/\Delta})]}\Sigma\Pi^{[t]}$ circuit of top fan-in at most $s^{O(d/t)}$ and size $s^{O(t+d/t)}$.*

The multiplication gates at the second layer of the resulting depth four circuit have a much larger fan-in than what is claimed in Theorem 2 or Theorem 6. When we begin with additional structure in the circuit, it seems we get additional structure in the resulting depth four circuit. Specifically, let us fix $t = \sqrt{d}$. The fan-in of the outer product gate would be $\Theta(\sqrt{d})$ for a general circuit (Theorem 2), $\Theta(\sqrt{d} \cdot \log d)$ for a homogeneous formula (Theorem 6), and $O(\sqrt{d} \cdot d^{1/100})$ for a circuit of depth 100 (Theorem 9).

Proof of Lemma 7. Let Φ be the product depth-Δ formula computing f. By Theorem 4, we get

$$f \quad = \quad \sum_{i=1}^{s} f_{i1} \cdot f_{i2} \cdots f_{ir} \tag{10}$$

with the required degree bounds. From the proof of Theorem 4, it follows that each f_{ij} is in fact a product of disjoint sub-formulas of Φ, and hence in particular f_{i1} is computable by size s formulas of product-depth Δ. We shall expand f_{i1} again to obtain the g_{ij}s.

Since f_{i1} is a polynomial of degree at least $d/3$ computed by a size s formula Φ' of product-depth Δ, there must be some multiplication gate h in Φ' of fan-in $\Omega(d^{1/\Delta})$. Therefore,

$$f_{i1} \quad = \quad A \cdot [h] \quad + \quad B.$$

Since B is computed by Φ' with $h = 0$, we can induct on B to obtain

$$f_{i1} \quad = \quad A_1[h_1] + \cdots + A_s[h_s]$$

where each h_i is a multiplication gate of fan-in $\Omega(d^{1/\Delta})$. Plugging this in (10), and replacing $[h_i]$'s by the factors, gives (8). □

References

[AJMV98] Eric Allender, Jia Jiao, Meena Mahajan, and V. Vinay. Non-Commutative Arithmetic Circuits: Depth Reduction and Size Lower Bounds. *Theoretical Computer Science*, 209(1-2):47–86, 1998.

[AV08] Manindra Agrawal and V. Vinay. Arithmetic circuits: A chasm at depth four. In *Foundations of Computer Science (FOCS)*, pages 67–75, 2008.

[FLMS14] Hervé Fournier, Nutan Limaye, Guillaume Malod, and Srikanth Srinivasan. Lower bounds for depth 4 formulas computing iterated matrix multiplication. In *Symposium on Theory of Computing (STOC)*, pages 128–135, 2014.

[GKKS13] Ankit Gupta, Pritish Kamath, Neeraj Kayal, and Ramprasad Saptharishi. Approaching the chasm at depth four. In *Conference on Computational Complexity (CCC)*, 2013.

[HY11] Pavel Hrubes and Amir Yehudayoff. Homogeneous formulas and symmetric polynomials. *Computational Complexity*, 20(3):559–578, 2011.

[Kay12] Neeraj Kayal. An exponential lower bound for the sum of powers of bounded degree polynomials. Technical report, Electronic Colloquium on Computational Complexity (ECCC), 2012.

[KLSS14] Neeraj Kayal, Nutan Limaye, Chandan Saha, and Srikanth Srinivasan. An Exponential Lower Bound for Homogeneous Depth Four Arithmetic Circuits. In *Foundations of Computer Science (FOCS)*, 2014.

[Koi12] Pascal Koiran. Arithmetic circuits: The chasm at depth four gets wider. *Theoretical Computer Science*, 448:56–65, 2012.

[KS14a] Neeraj Kayal and Chandan Saha. Lower Bounds for Depth Three Arithmetic Circuits with small bottom fanin. *Electronic Colloquium on Computational Complexity (ECCC)*, 2014.

[KS14b] Mrinal Kumar and Shubhangi Saraf. The limits of depth reduction for arithmetic formulas: it's all about the top fan-in. In *Symposium on Theory of Computing (STOC)*, pages 136–145, 2014.

[KS14c] Mrinal Kumar and Shubhangi Saraf. On the power of homogeneous depth 4 arithmetic circuits. In *Foundations of Computer Science (FOCS)*, 2014.

[KSS14] Neeraj Kayal, Chandan Saha, and Ramprasad Saptharishi. A super-polynomial lower bound for regular arithmetic formulas. In *Symposium on Theory of Computing (STOC)*, pages 146–153, 2014.

[Sap15] Ramprasad Saptharishi. A survey of known lower bounds for arithmetic circuit complexity. Github survey, http://github.com/dasarpmar/lowerbounds-survey/releases/, 2015.

[Tav13] Sébastien Tavenas. Improved bounds for reduction to depth 4 and depth 3. In *Mathematical Foundations of Computer Science (MFCS)*, pages 813–824, 2013.

[VSBR83] Leslie G. Valiant, Sven Skyum, S. Berkowitz, and Charles Rackoff. Fast Parallel Computation of Polynomials Using Few Processors. *SIAM Journal of Computing*, 12(4):641–644, 1983.